

Final Project Goals

1. Experience working on a larger project using a mixture of custom components and "IP": Some design experience can only be gained by experience working on larger scale projects with multiple components
2. Experience working in a team setting
3. Project documentation and defense

Requirements

1. Students are to organize in groups of 2-3.
2. The project should be suitably complex and interesting -- the example projects below can serve as a guide here, and the instructors can help to appropriately frame your project idea. The project must be approved by the instructors.
3. Your FPGA design should be a compartmentalized design so you can have each student in the group be responsible for design components.
4. The design should make use of "IP", in the form of ready-made components (i.e. CoreGen, Picoblaze) modifiable reference designs (such as design examples given by the instructors), as well as your own custom VHDL.
4. On the last day of class, groups will demonstrate the projects in front of the class, detail their design in presentation format, and answer questions from classmates and instructors.

The biggest requirement is that you make something fun, and learn about FPGA design in the process.

Project Component Suggestions

Through the rest of the class, we will be doing short labs and exercises with some of the other interfaces on the board. Using these in your project will allow you to leverage the capability that you will get from each of these mini-labs. These pieces include:

1. Use of the USB port on the NEXYS2 board to provide a high speed data link between the PC and your FPGA design.
2. 1-bit DAC (Digital to Analog Converter) for playing audio to headphones or speakers.
3. A DDS for tone synthesis
4. Interfacing to external memory on the NEXYS2 board.

Furthermore, sample code can be obtained which demonstrates:

1. VGA image display
2. PS/2 (old-style) mouse and keyboard interface

Example Projects

1) A Digital Picture Frame:

1. Loads up to 4 images over the high-speed USB into external memory
2. Accepting commands from the push-buttons, a user can select to display a "small" version of all four images tiled on the screen
3. The user can use the mouse to select the image to display full-size from the four tiles
4. Supports a slide-show mode with simple image transitions (fade-in/out, etc.)

2) An "MP3" player:

1. Download .wav files over the high-speed USB into external memory
2. Switch definitions that allow a user to
3. Each .wav file has a name which scrolls across the 7-segment displays, allowing the user to select the song using the push-buttons to go "up" and "down" the playlist
4. Support an arbitrary waveform generator, where a user can also select to play a sine wave or a square wave with a user selected frequency. The frequency would be printed to the seven-segment displays.

Schedule

The project development schedule is flexible, but you are encouraged to get started early, using the lab time in class when possible. The instructors will be there to assist each week, and there are oscilloscopes and computers available for the teams. Initial project proposals and group organizations will be due next week, and the CDR will be due the week after that (4/20/09). The instructors reserve the right to reorganize groupings, and mandate extra features!

Critical Design Review (CDR) (4/20/09)

An in-class (less than 10 minutes) presentation (PowerPoint or other) which will include:

1. Description of project
2. Team members and their responsibilities
3. Block diagram and estimate of device resource utilization (i.e., block RAM, rough estimate of registers used, and I/O pins)
4. External components used
5. VHDL development to date
6. Schedule, risks, and risk mitigation

Project Defense (5/04/09)

An in-class (less than 10 minutes) presentation which will include:

1. Description of project
2. Team members and their responsibilities
3. Block diagram, and summary of resource utilization
4. Presentation of each sub-project by team members (each team member must present). This should summarize the design, any challenges encountered, and include a demonstration.

Website

An externally hosted (i.e. googlepages, yahoo or other web site hosting place) webpage(s) which contains the presentations (CDR, Final). It should also include:

1. description
2. Link to the complete project archive in .zip format
3. Link to the project bitfile
4. Link to any additional software required to operate your design (for example, if you build a simple piece of software for the PC)
5. Link to the synthesis report
6. Any other documents relevant to your project