VHDL/FPGA Microprocessor Design
525.442
Assignment 3

Introduction

This lab will create a test interface to the 16 MB Cellular RAM available on the Nexys2 board. Your design will load the first 256 memory locations with a preset pattern, and then will allow a user at the board to check the memory values on the seven segment display using the slider switches and push buttons.

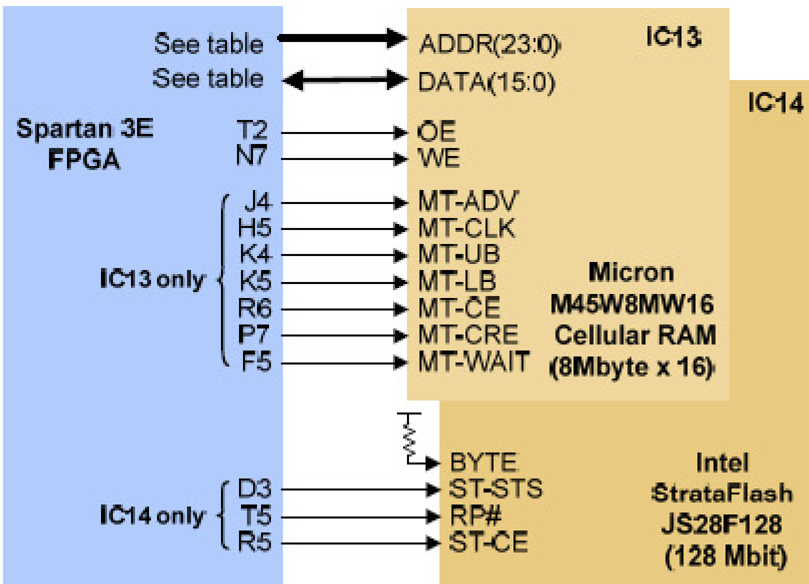

Figure 1: Cellular RAM and Flash attached to the Spartan FPGA.

Task 1

Upon asynchronous reset (BTN3), the VHDL design will load the first 256 locations of external memory with the pattern 0xA5[address]. For example:

Address	Data Value
0x00	0xA500
0x01	0xA501
0x02	0xA502
	…
0xFF	0xA5FF

Figure 2: Data values for each memory address from 0x00 to 0xFF.

As illustrated in Figure 3, writing data to external memory upon reset requires the write operations to be synchronously sequenced (this is mainly because the Nexys2 has a 20 ns clock period, and the memory takes 70 ns per access). Figure 3 gives a potential approach to synchronously sequence our write logic using a circular shift register with only 1-bit high to represent the current "state" of the operation. In this illustration, the 5 different portions of the write cycle are each represented by a 1 in a particular flip-flop of the shift register.

Note that your design can be different. If you would like to improve upon this outline in subtle ways, feel free, and if you would like to consider a different approach completely, feel free.

Let's consider this outline a bit more. When the first bit of the shift register is high, the data and address counters are both incremented. During this time, the CE# and WE# are both high.

When the second bit of the shift register is high, the CE# and WE# are asserted, starting the write operation. Although the data is not required to be valid at this point, in this design it will be. Note that LB# and UB# can be held low during the entire operation – they do not need to be cycled like CE# and WE#.

When the third bit and fourth bit of the shift register are high, the CE# and WE# continue to stay asserted. This allows our design to meet the 70 ns write cycle time.

During the period when the fifth bit is high, the data will be latched by the SRAM.

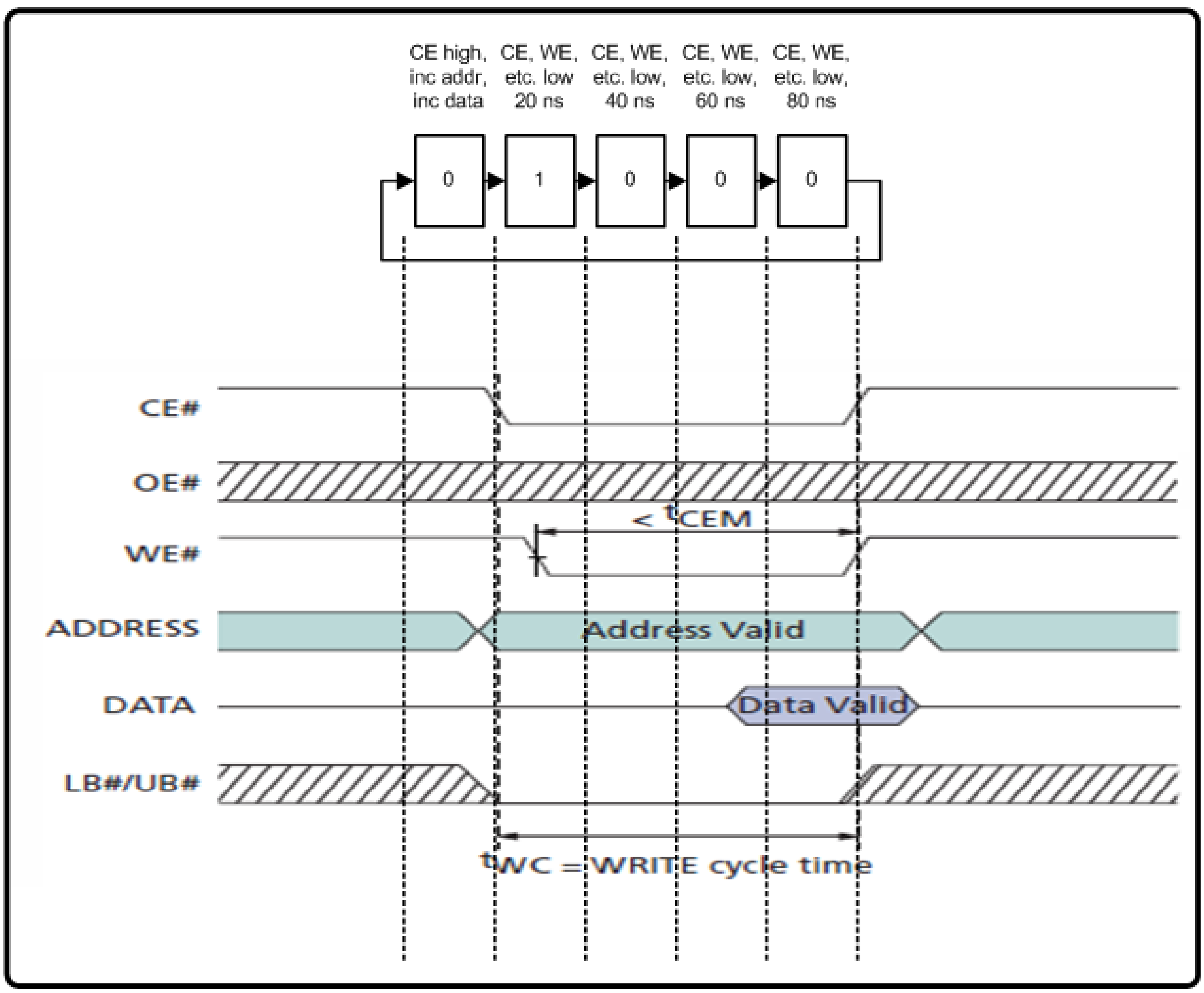

Figure 3: Data write sequencing. By starting with the 1 in the second location, the address and data are only incremented after the first write, simplifying the reset condition.

Task 2
After the data is loaded, the user should be able to read the values stored in memory. The slider switches will set the current address to read from. Pressing BTN0 should perform a memory read. The result of the last read should be displayed on the seven segment display *unless* the user is pressing BTN1, then the current address on the slider switches should be displayed.

Note that the read signals (CE# and OE#) must be asserted for less than 4 us. Thus, when a user presses BTN0, a signal synchronous to the 50 MHz clock should be generated to assert CE#, OE#, and WE# for an appropriate amount of time. A block diagram of possible hardware to accomplish this is given below.

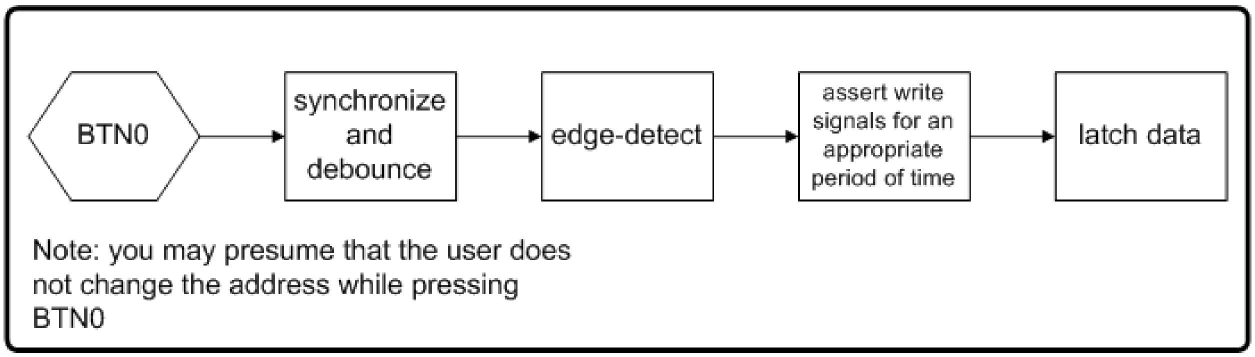

Figure 4: Block diagram for reading memory.

Task 3
Build a simple testbed to supply a clock and a reset to your design. Simulate your design loading memory after reset. Zoom in on the second memory write (memory address 0x01) and the second to last memory write (memory address 0xFE). Save a screen capture of both of these in a file – they must be submitted with your electronic submission as well as with your paper copy of your VHDL.

Some Notes
1) Your implemented design should only be two VHDL files, a top level file and your seven segment display. Your top level file should only include one entity/architecture pair. In addition, you should have a third testbench VHDL file.

2) The datasheet for the memory is:
http://download.micron.com/pdf/datasheets/psram/128mb_burst_cr1_5_p26z.pdf

3) The data bus is bidirectional. You will need to tri-state the bus after you are done writing to the memory – see the tri-state example in the second lecture.

To Turn In
1) Readable paper copies of:
   a. appropriately commented VHDL for the top level VHDL file;
   b. the VHDL for the simple testbench;

c. printouts of the two screen captures from the test bench;
d. printout summarizing your synthesis results.

2) The zipped project directory (lab3_yourlastname.zip) and the bit file (lab3_yourlastname.bit) via the submission link on the webpage. This must be turned in by 4:25 on the day of class. The project directory should include the electronic version of the paper submission.
3) Bring your board with the assignment loaded into the non-volatile memory so that all that is required to demo the assignment is simply powering the board. An instructor will check for correct operation during the lab period

Grading Sheet

20 points
DEMO: Memory appears to be correctly loaded by the write operation.

20 points
DEMO: BTN0 reads memory.

5 points
DEMO: When BTN1 is depressed, the current address on the switches is displayed

5 points
DEMO: Switches choose the address to read.

5 points
DEMO: BTN3 asynchronously resets the design.

20 points
Screenshots of the testbench execution appear correct.

25 points
Quality of VHDL code and hardware design and summary of synthesis results. Graded from printed copies submitted in class.