VHDL/FPGA Microprocessor Design
525.442
Assignment 4

Introduction
This lab will create a design to demonstrate using the VGA controller on the Nexys2 board. The design will utilize a VHDL VGA interface module provided by Digilent to control the VGA port, and will create a checkerboard pattern on an attached monitor with a highlighted square that can be moved by the buttons.

Task 1
Develop a block diagram of the VGA interface module. Before using the block diagram, you should understand its operation by creating a simple block diagram of its VHDL code. The block diagram should be similar in complexity to those presented in class for homework solutions. This block diagram can be hand-drawn, and should be turned in with your VHDL code developed for Task 2.

Task 2
Below is an image of the VGA output expected for this lab. Using theVGA interface module, create a "checkerboard" pattern with 20 columns and 15 rows. The blocks should alternate green, blue, green, etc., as shown in the picture.

In addition, one block should be highlighted red. The red highlighted block can be moved by the pushbuttons around the screen.

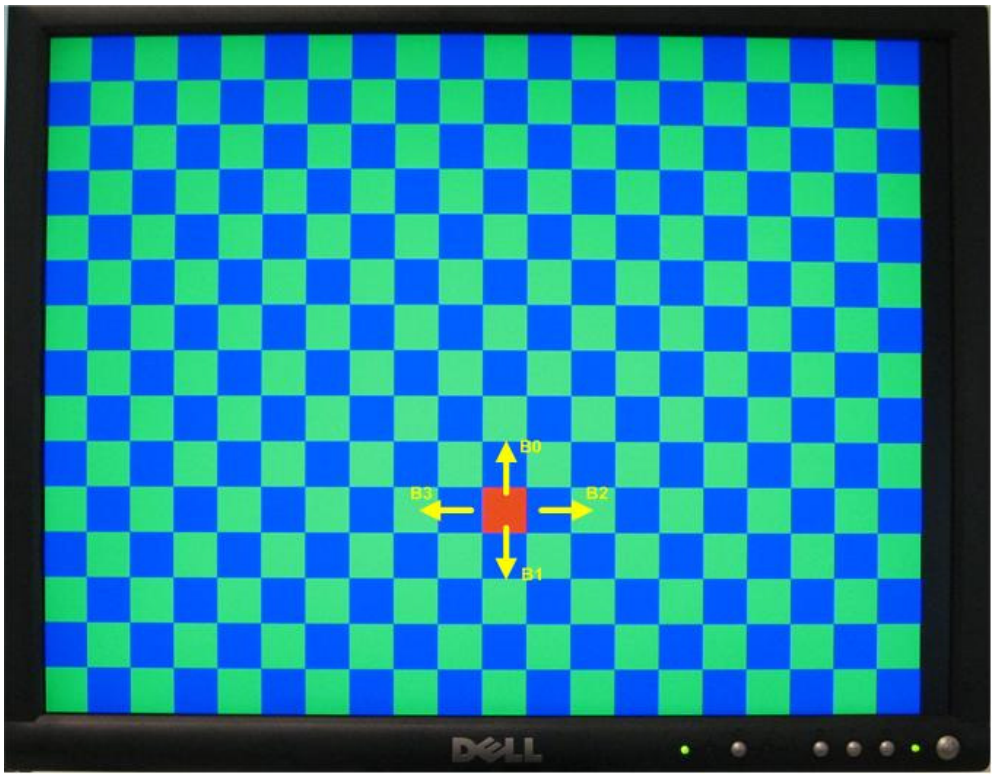

Figure 1: Image of the lab assignment VGA output.

If the highlighted block reaches an edge of the screen, it should wrap around to the other edge.

In addition to highlighting the screen, a light should blink from LED0 to LED7 (and then loop back to LED0), moving from one LED to the next each second. Describing this a different way, a light should "walk" across the LEDs at a rate of one LED per second (only one LED should be highlighted at any time) and should loop around when the edge is reached. The timing for this should be derived from the VGA timing. That is, since you know that the screen is rewritten 60 times per second (since the refresh rate of the module is 60 Hz), you should move the LED every time the screen is refreshed 60 seconds.

Switch0 will be used as a reset.

A summary of the expected inputs and outputs.

Users Inputs
Switch0: Active high reset.
Button0: Move the highlighted block up. The block should only move once for each button press.
Button1: Move the highlighted block down. . The block should only move once for each button press.
Button2: Move the highlighted block right. . The block should only move once for each button press.
Button3: Move the highlighted block left. . The block should only move once for each button press.

Outputs
VGA Port: See Figure 1.
LEDs: A light should walk across the LEDs at the rate of one LED per second. The timing should be derived from the timing created by the VGA module.

Task 3
Simulate your VGA demonstration. Create a screenshot of the simulation over the time period where the first row is created by your VGA module.

Some Notes
1) Your implemented design should only be one VHDL file, not including the provided VGA module. The top level file should only include one entity/architecture pair. In addition, you should have a testbench VHDL file.
2) Read the section in the Nexys2 manual describing the operation of the VGA module before beginning this lab!

To Turn In

1) Readable paper copies of:
    a. Your block diagram of the VHDL VGA interface module;
    b. appropriately commented VHDL for the top level VHDL file;
    c. the VHDL for the simple testbench;
    d. printouts of the screen capture from the test bench;
    e. printout summarizing your synthesis results.
2) The zipped project directory (lab4_yourlastname.zip) and the bit file (lab4_yourlastname.bit) via the submission link on the webpage. This must be turned in by 4:25 on the day of class. The project directory should include the electronic version of the paper submission.
3) Bring your board with the assignment loaded into the non-volatile memory so that all that is required to demo the assignment is simply powering the board. An instructor will check for correct operation during the lab period.

Grading Sheet

5 points
Block diagram of VGA interface.

20 points
DEMO: VGA checkerboard display is correct

10 points
DEMO: Red block is displayed on reset at the reset location.

10 points
DEMO: Red block is moved by button presses. Box only moves one block for each button press.

5 points
DEMO: Red block correctly wraps at the screen edges.

5 points
DEMO: Switch0 resets the design.

10 points
Screenshot of the testbench execution appear correct.

10 points
DEMO: LEDs scroll as described in the lab.

25 points
Quality of VHDL code and hardware design and summary of synthesis results. Graded from printed copies submitted in class.