

COVER PAGE

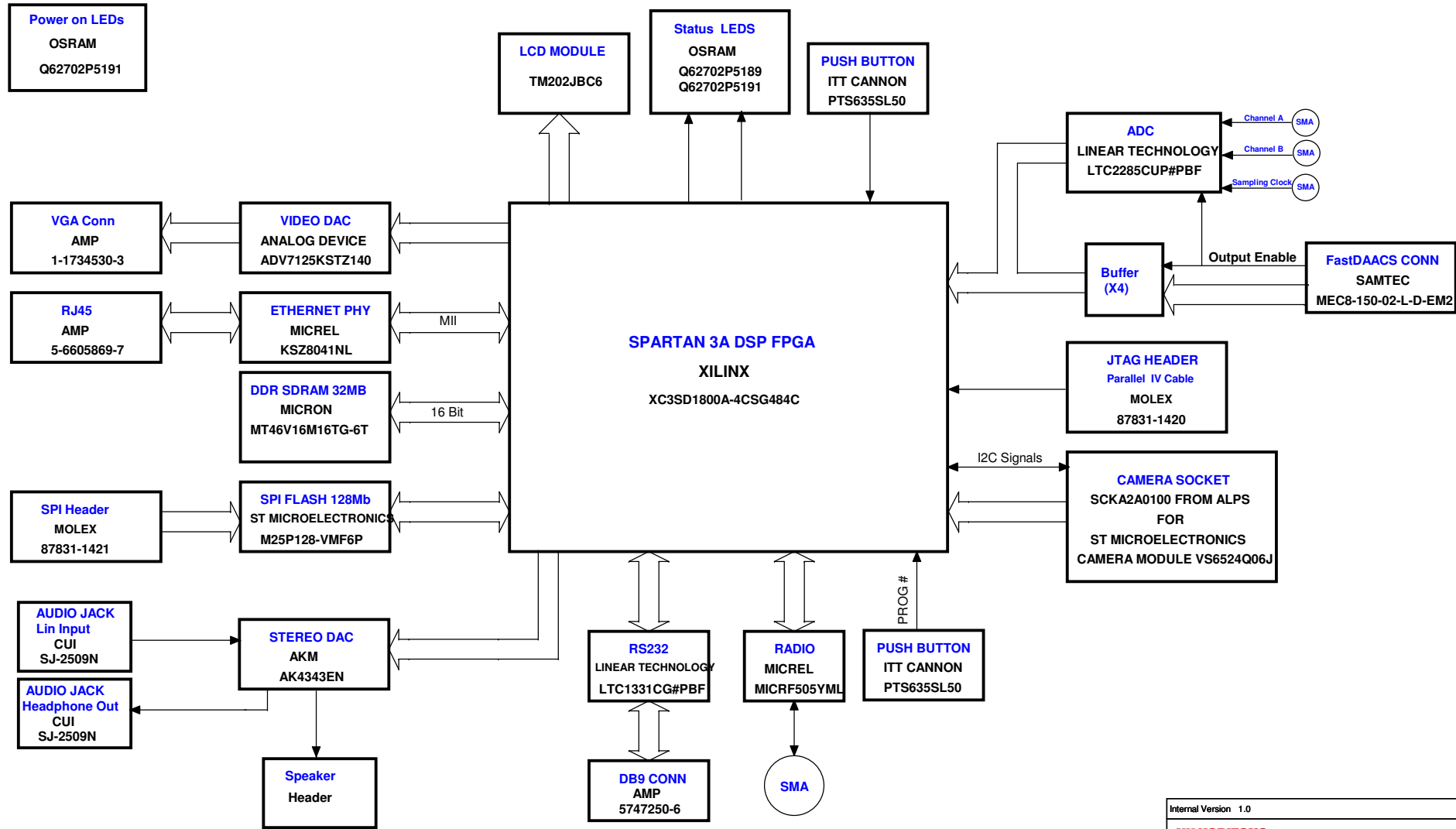
SPARTAN 3A DSP REFERENCE KIT

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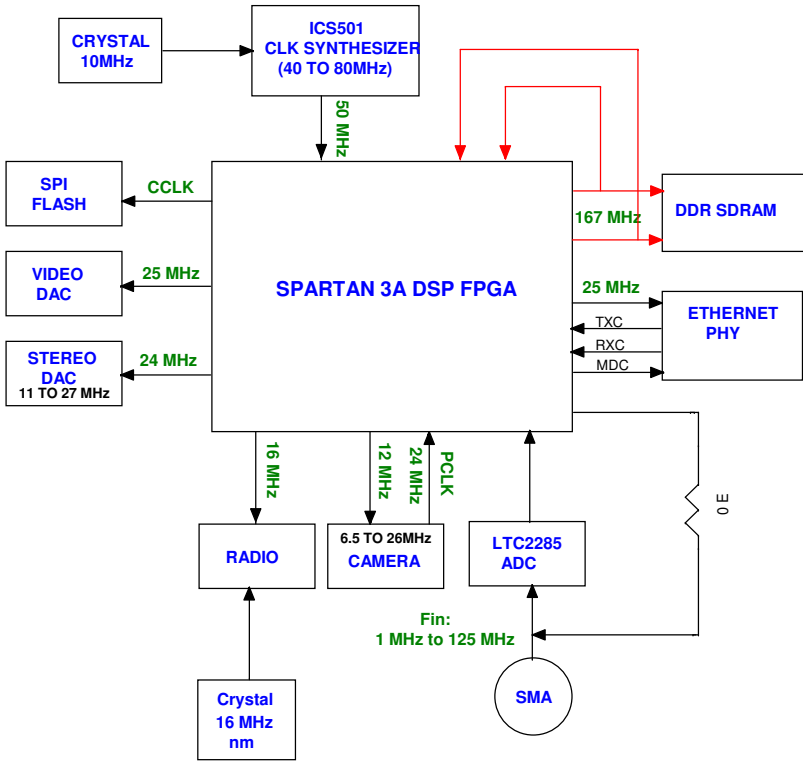
BLOCK DIAGRAM



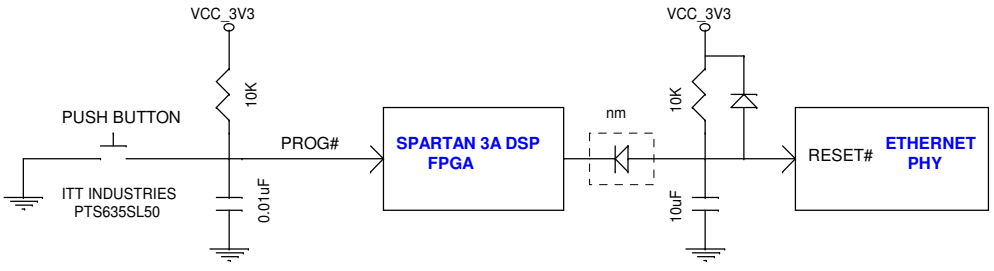
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CLOCK & RESET SCHEME

CLOCK SCHEME

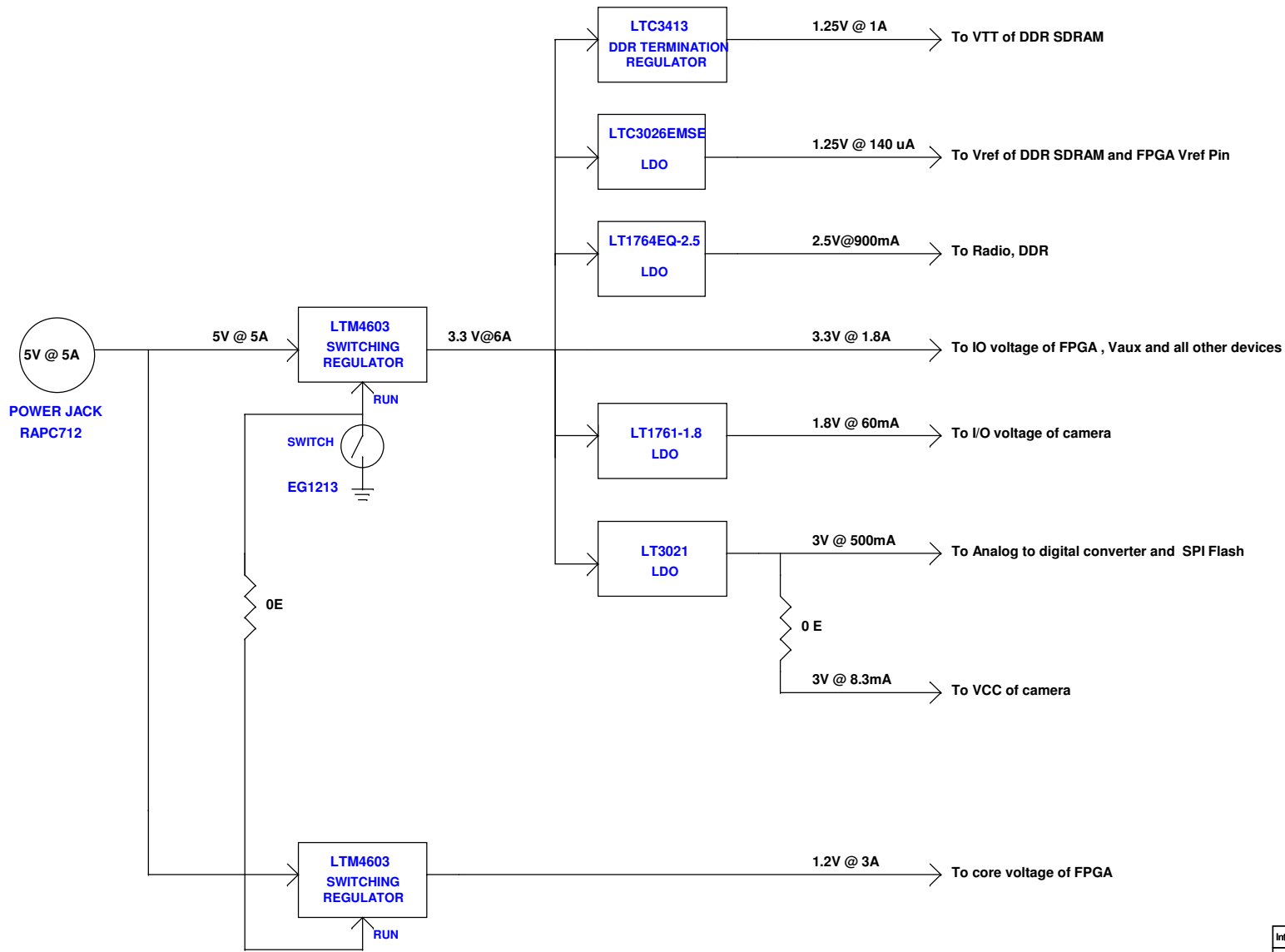


RESET SCHEME



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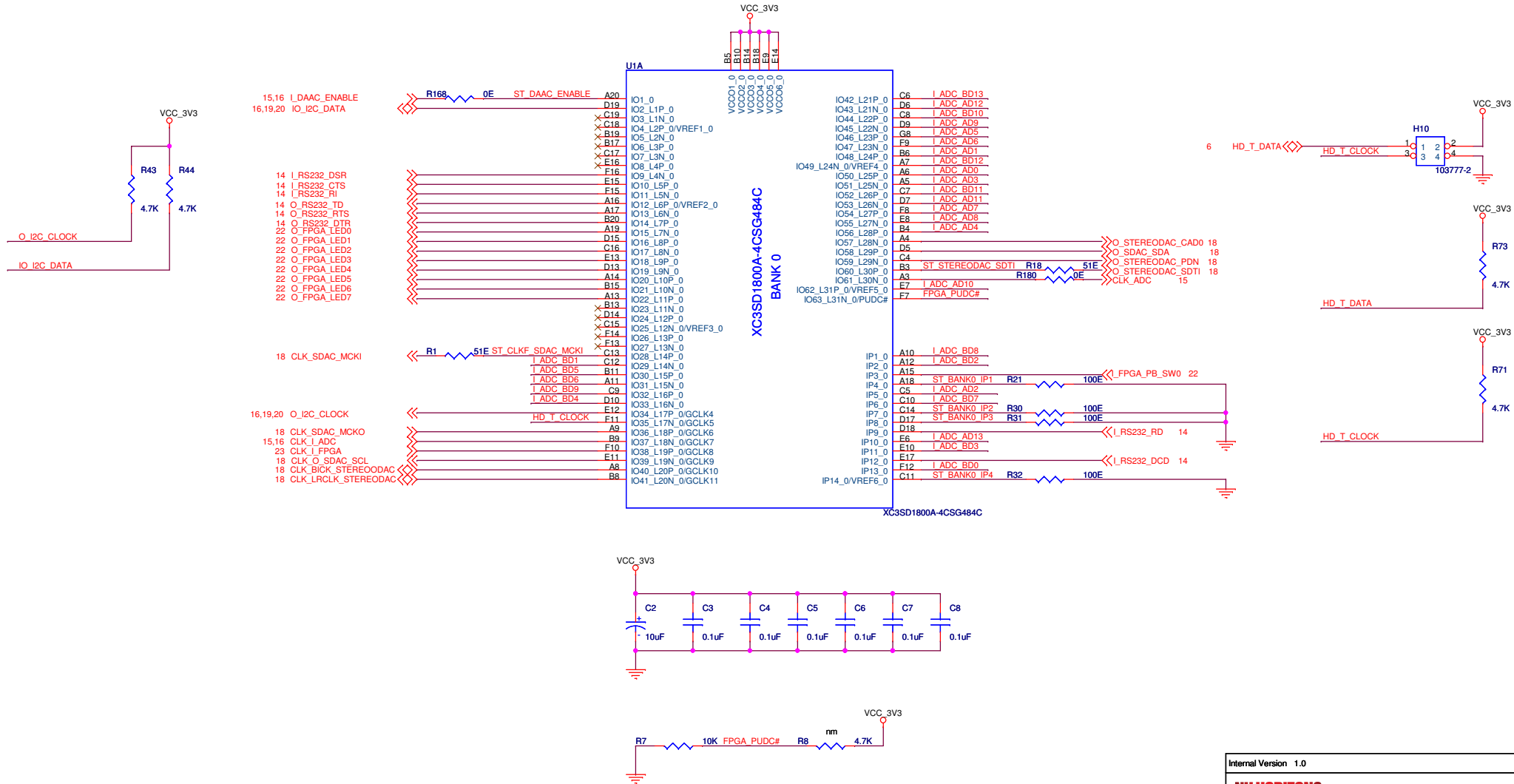
POWER SCHEME



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15,16 I_ADC_AD[0:13] >>
 15,16 I_ADC_BD[0:13] >>

SPARTAN 3A DSP BANK 0

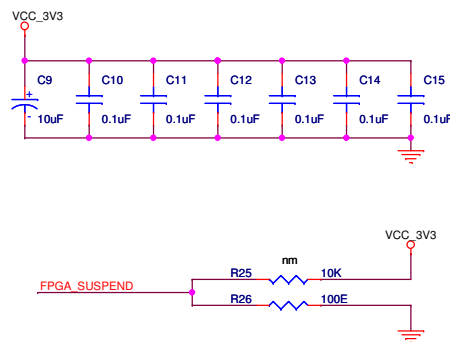
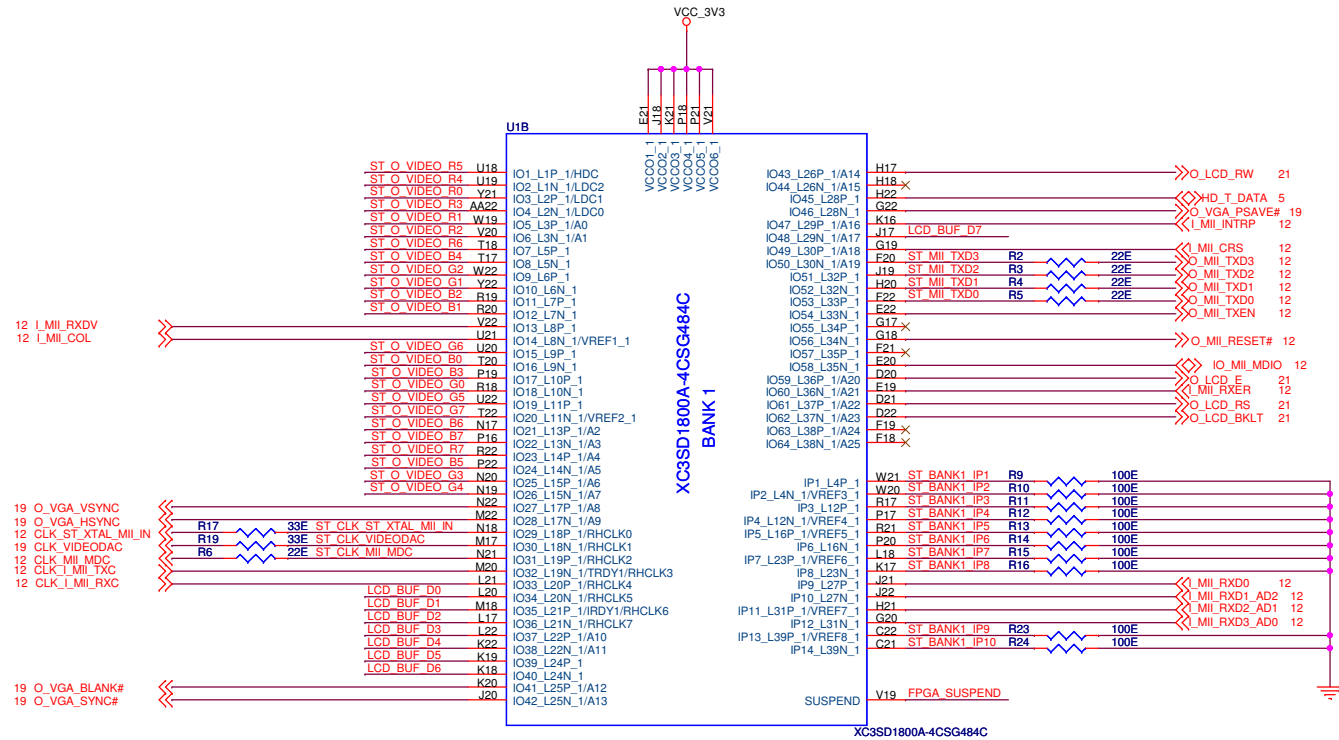


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SPARTAN 3A DSP BANK 1

21 LCD_BUF_D[0:7]

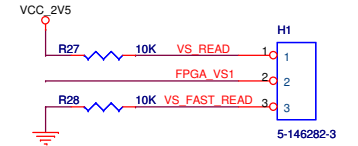
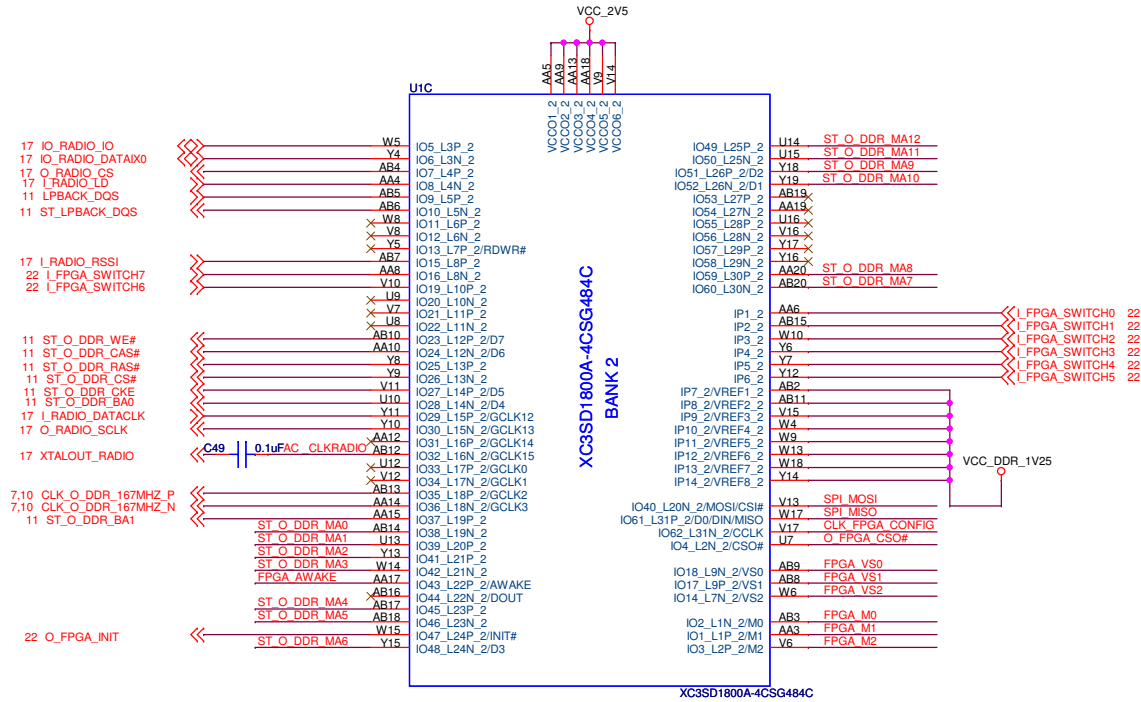
ST_O_VIDEO_R[0:7] 19
 ST_O_VIDEO_G[0:7] 19
 ST_O_VIDEO_B[0:7] 19



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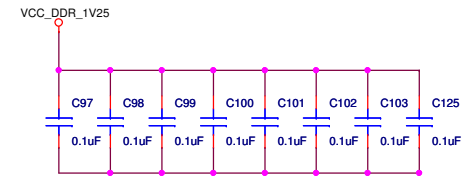
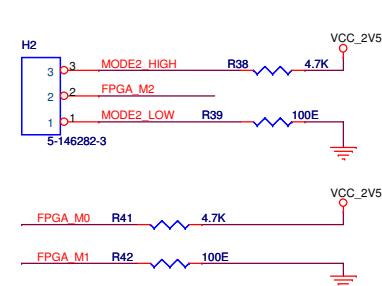
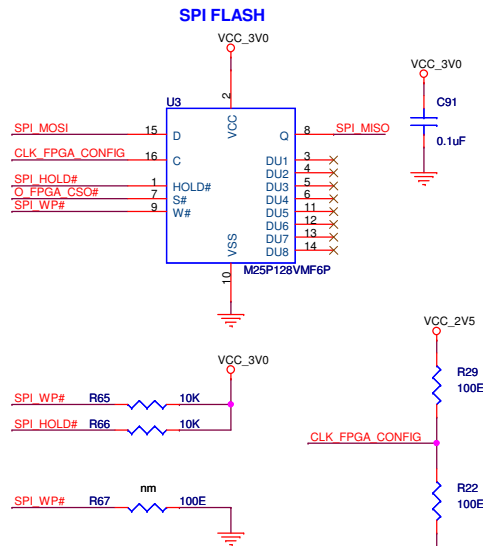
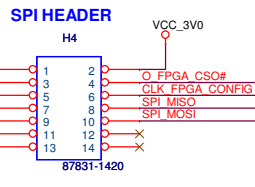
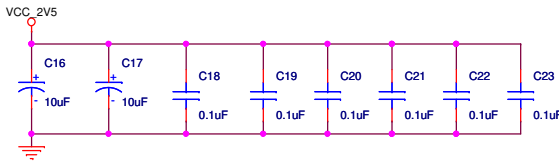
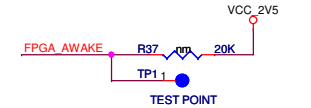
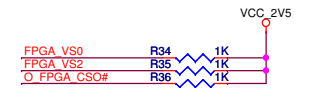
SPARTAN 3A DSP BANK 2

ST_O_DDR_MA[0:12] 11



JUMPER SETTING OF H1

JUMPER SETTING	SPI READ COMMAND	VS0	VS1	VS2
1-2	FAST READ (0X0B)	1	1	1
3-2	READ (0X03)	1	0	1



SPARTAN 3A CONFIGURATION MODE

CONFIGURATION MODE	M2	M1	M0	DATA WIDTH
JTAG *	1	0	1	1Bit
SPI	0	0	1	1Bit

* Default

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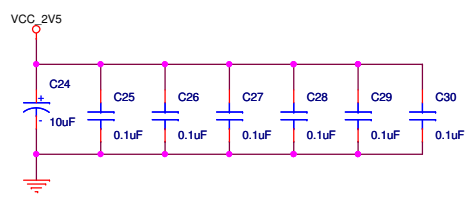
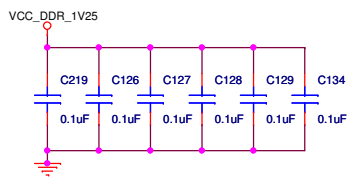
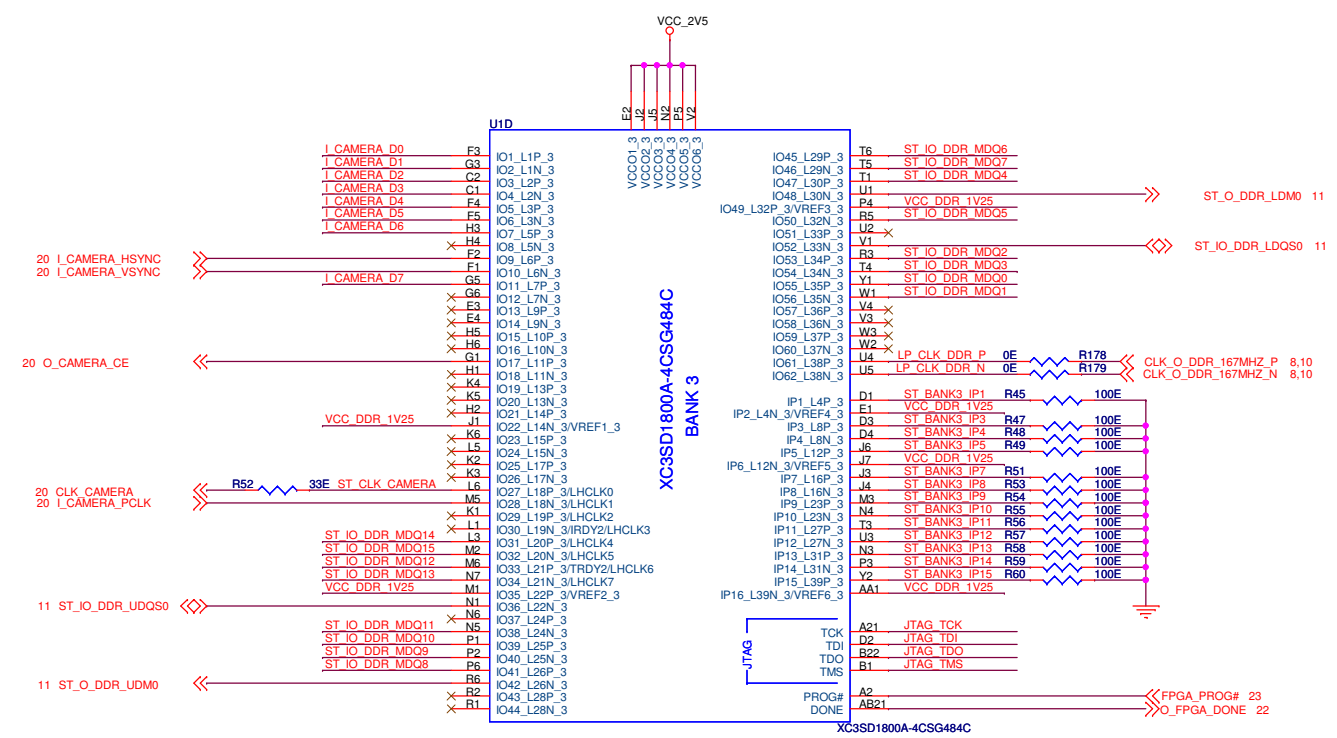
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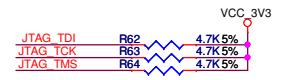
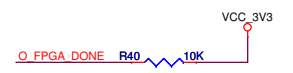
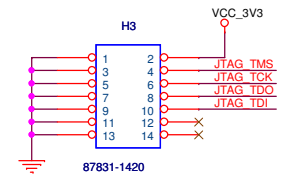
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SPARTAN 3A DSP BANK 3

20 L_CAMERA_D[0:7] >>
 11 ST_IO_DDR_MDQ[0:15] <<

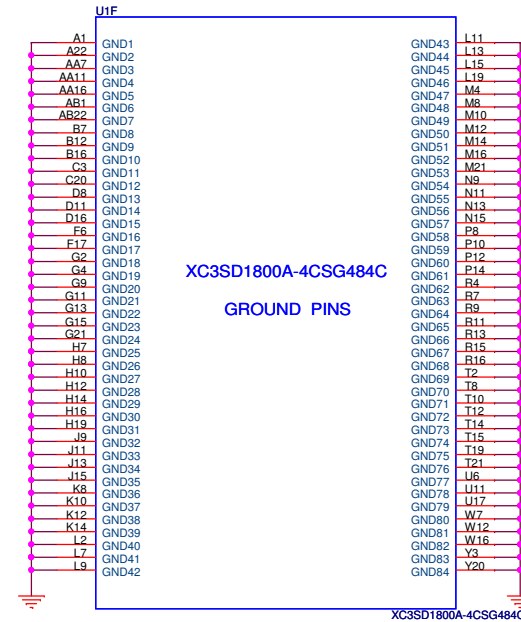
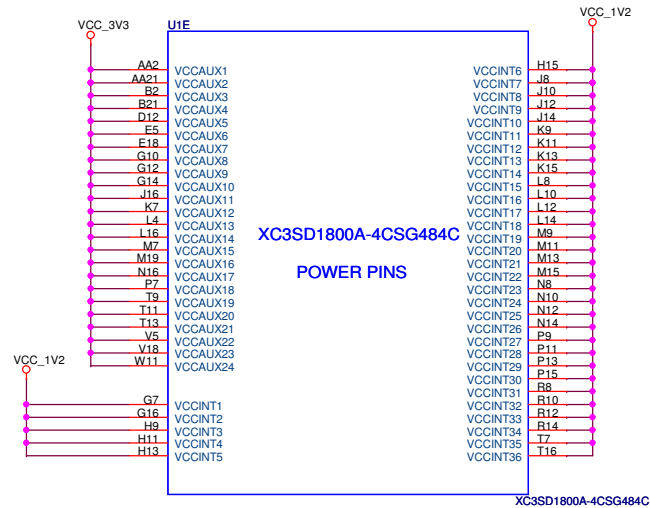


PARALLEL IV JTAG

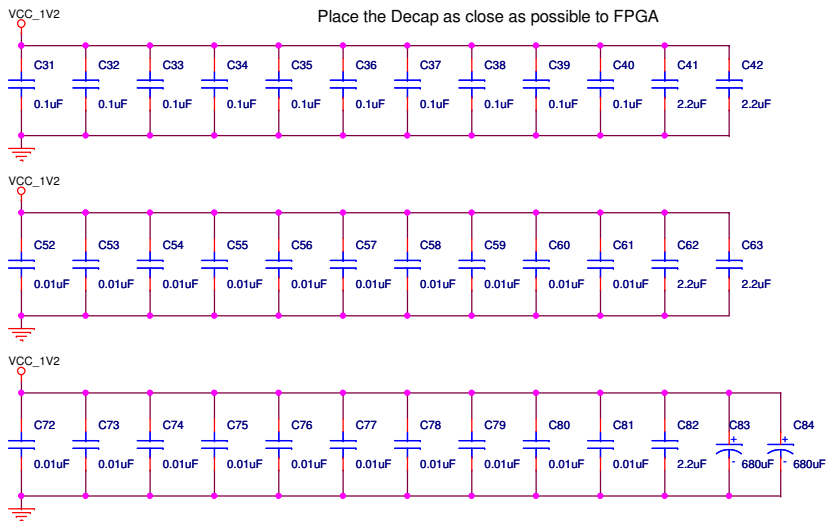


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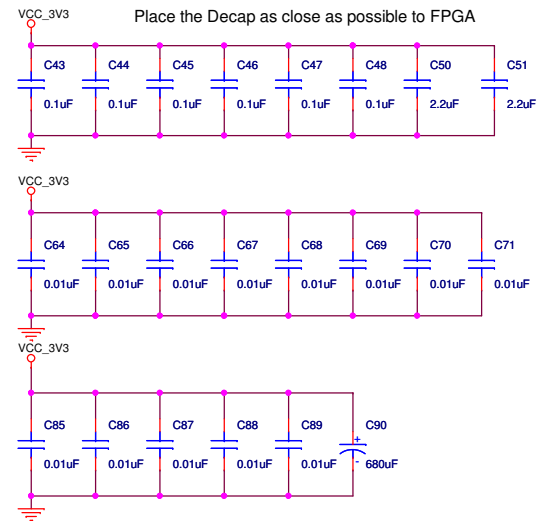
SPARTAN 3A DSP POWER



Decap for VCCINT



Decap for VCCAUX



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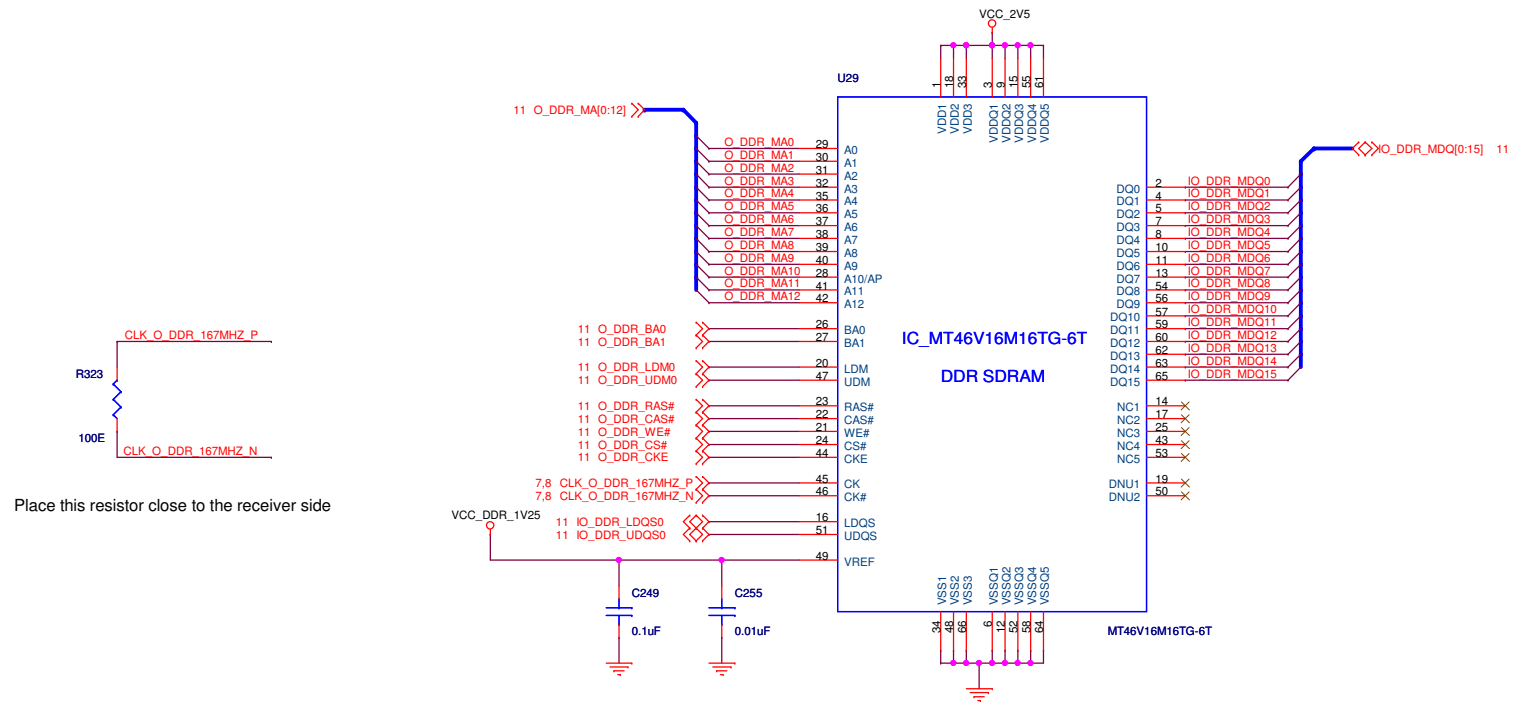
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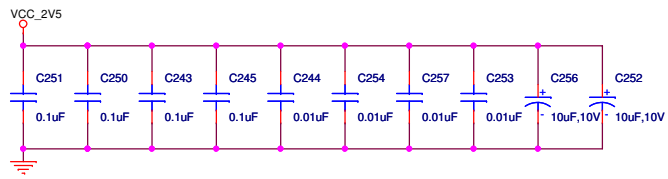
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DDR SDRAM



Place this resistor close to the receiver side



DATA BUS MASK	DATA BUS STROBE	DATA BUS
LDM0	LDQS0	DQ[0-7]
UDM	UDQS0	DQ[8-15]

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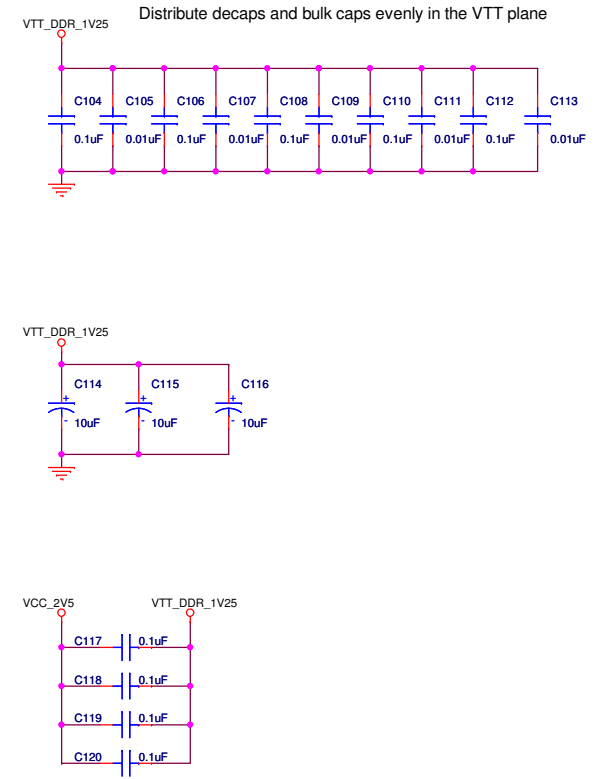
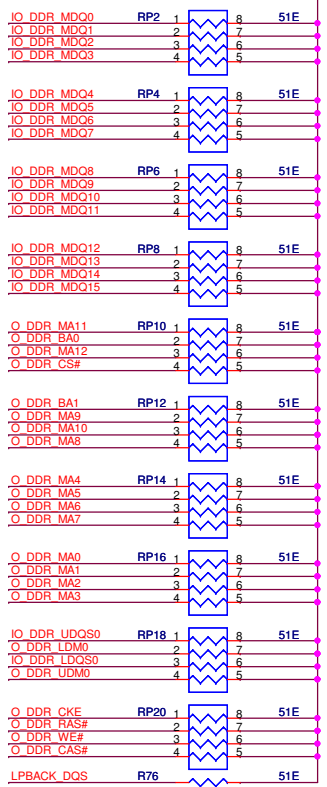
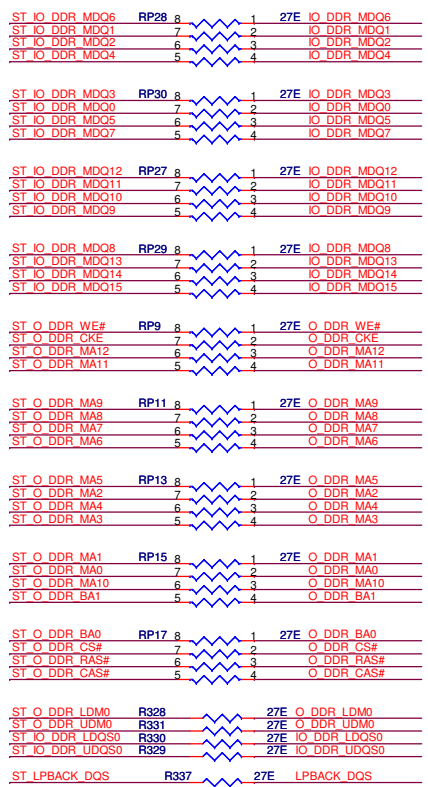
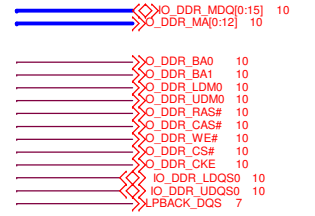
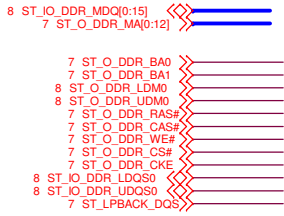
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Title: DDR SDRAM

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DDR TERMINATION



MII ETHERNET

Strapping Options

nm	m	Isolate
R94	R85	Enable
R85	R94	Disable*

* - Default

nm	m	Speed
R86	R92	100 Mbps*
R92	R86	10 Mbps

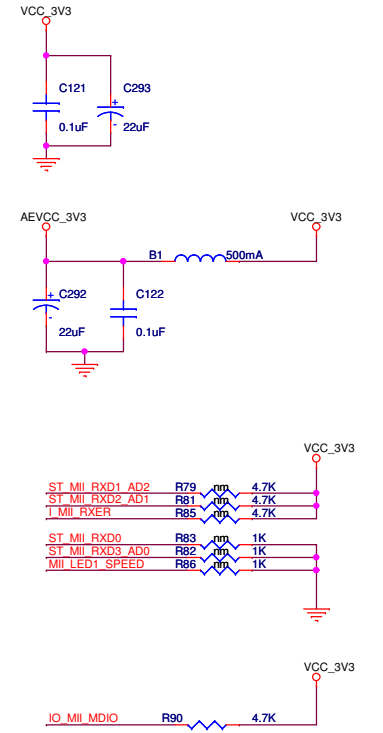
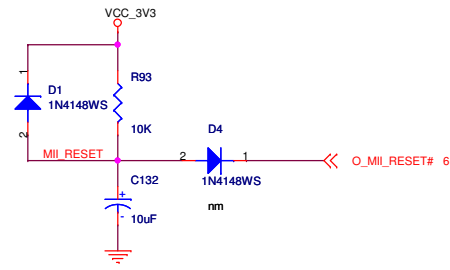
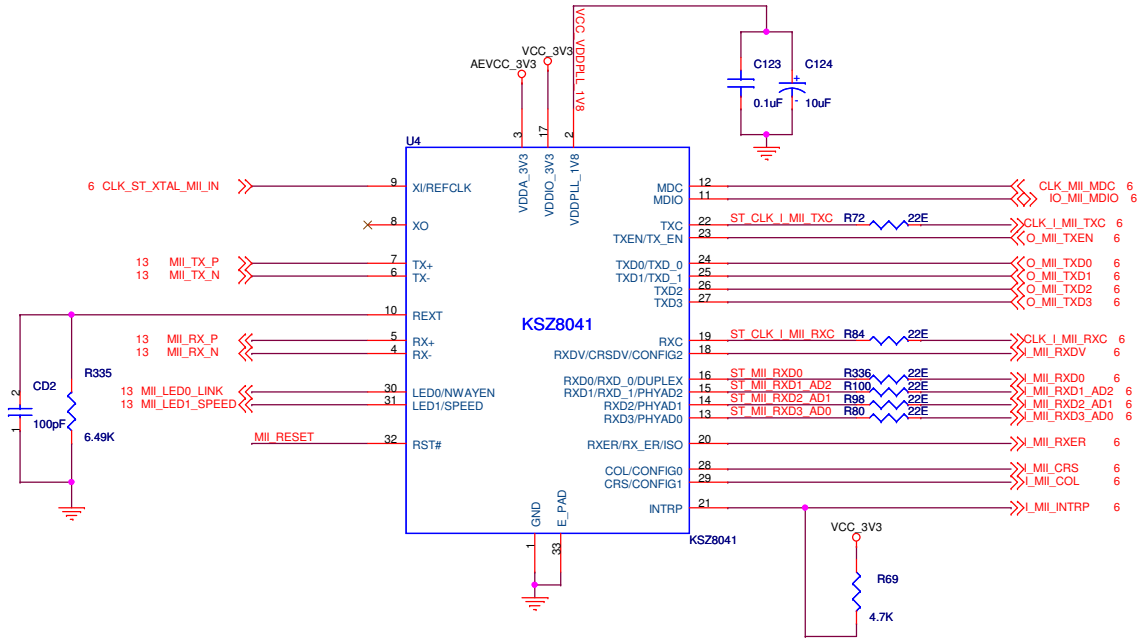
* - Default

nm	m	Duplex
R83	R87	Half Duplex*
R87	R83	Full Duplex

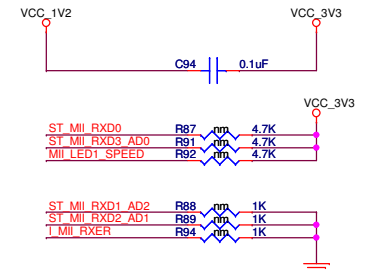
* - Default

nm	m	Phy Address
R79 , R81 , R91	R87 , R89 , R82	00000
R79 , R81 , R82	R87 , R89 , R91	00001*
R79 , R89 , R91	R87 , R81 , R82	00010
R79 , R89 , R82	R87 , R81 , R91	00011
R87 , R81 , R91	R79 , R89 , R82	00100
R87 , R81 , R82	R79 , R89 , R91	00101
R87 , R89 , R91	R79 , R81 , R82	00110
R87 , R89 , R82	R79 , R81 , R91	00111

Default Phy Address : 00001*



Stitching Cap



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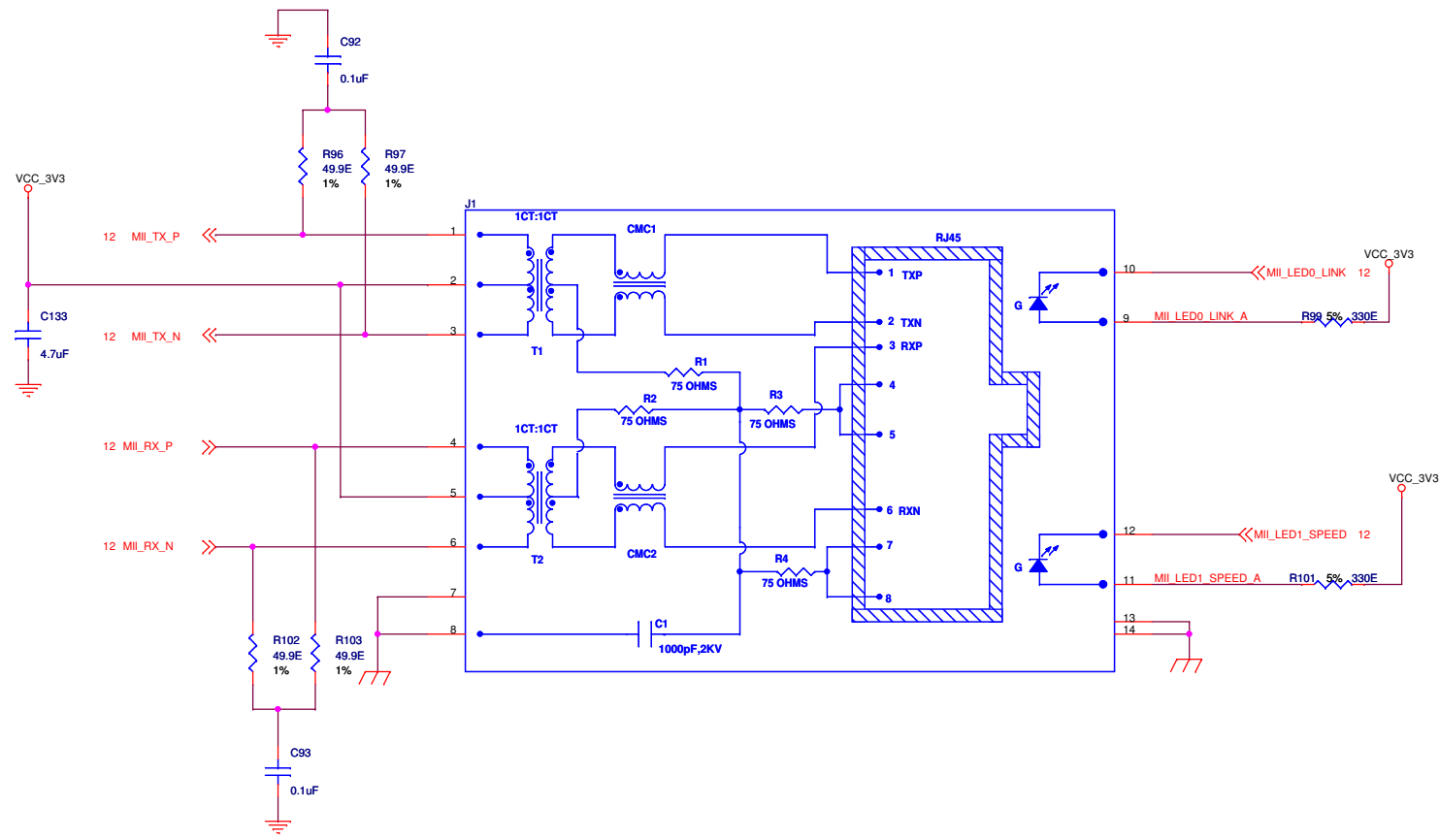
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Title: MII ETHERNET

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RJ45 CONNECTOR

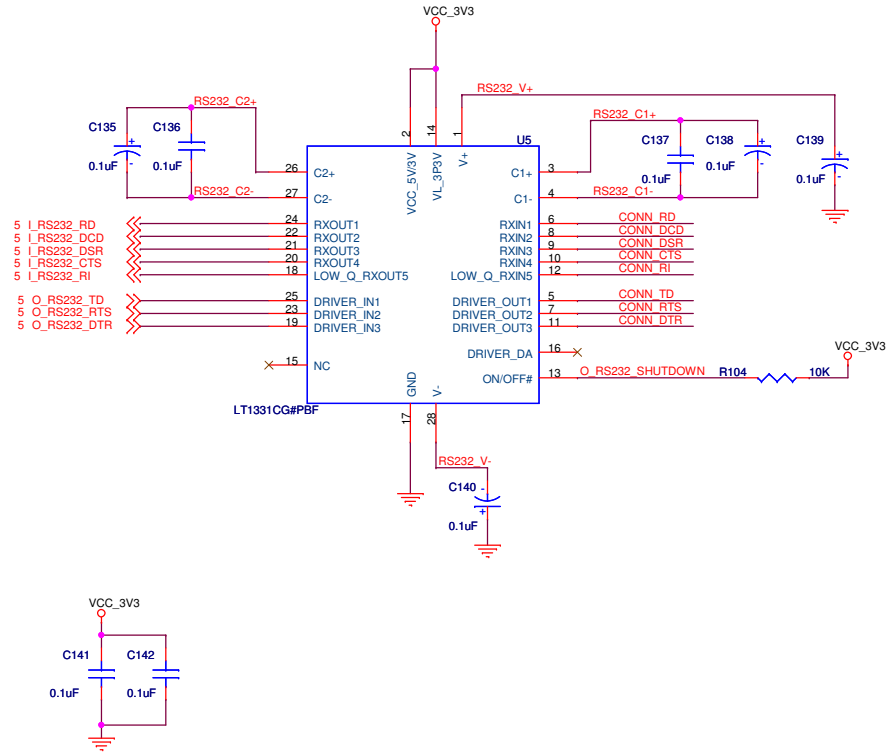


R96 , R97 , R102 and R103 should be placed near to the PHY

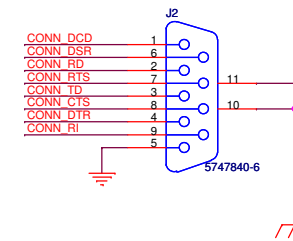
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RS232 TRANSCEIVER

RS232 TRANSCEIVER



DB9 CONNECTOR

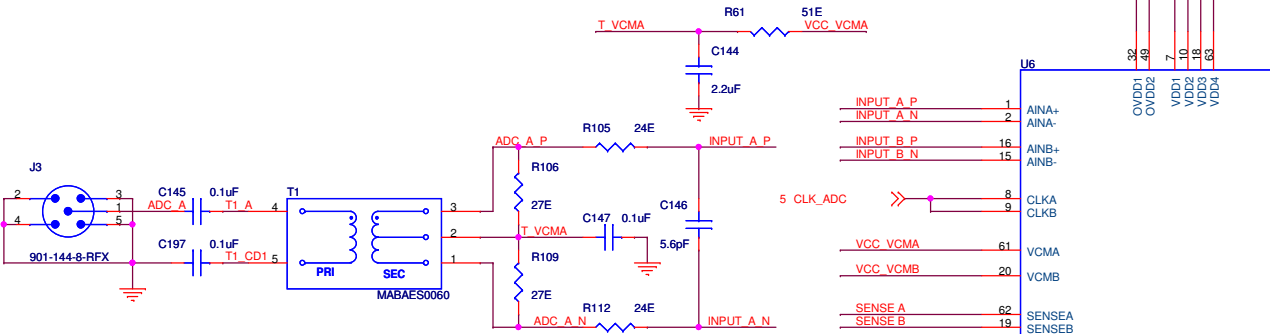
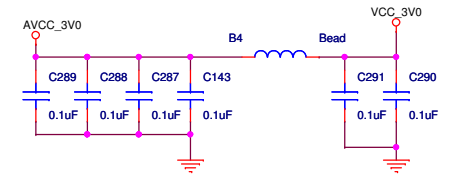


Cross Over Cable is used for connecting this to PC port

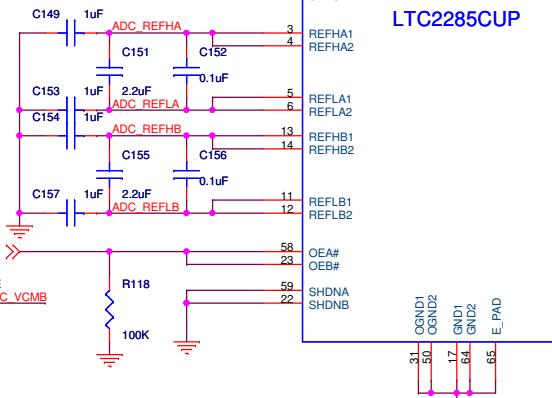
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A/D CONVERTER

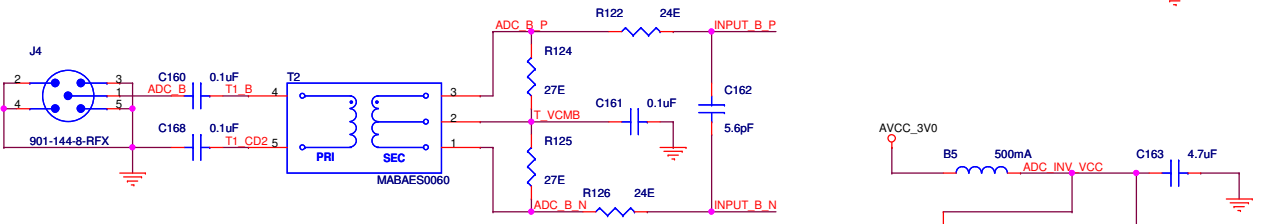
C144 and c158 should be placed near the corresponding VCM* pins



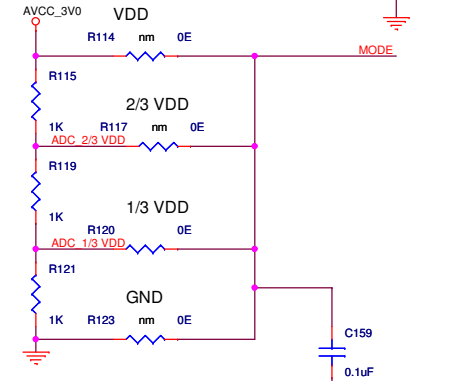
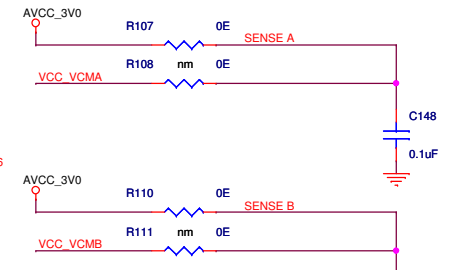
INPUT_A_P and INPUT_A_N should be routed in differential pair



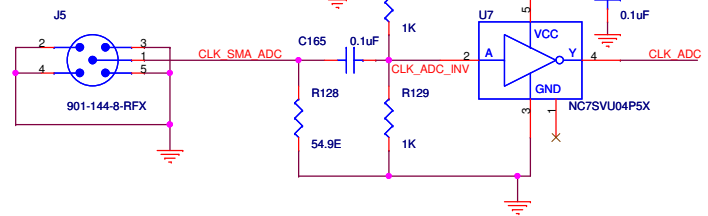
C146 AND C162 should be close to ADC as possible



INPUT_B_P and INPUT_B_N should be routed in differential pair



SHDNA SHDNB	OEA# OEB#	Output Mode
0	0	Normal Operation
0	1	Normal Operation Output Hi-Z
1	0	Nap Mode Output Hi-Z



CLK_ADC can also be given from FPGA

MODE	OUTPUT FORMAT	CLOCK DUTY CYCLE STABILISER	Resistor	
			m	nm
0	OFFSET BINARY	OFF	R123	R120, R117, R114
1/3 VDD*	OFFSET BINARY	ON	R120	R123, R117, R114
2/3 VDD	2'S COMPLEMENT	ON	R117	R123, R120, R114
VDD	2'S COMPLEMENT	OFF	R114	R123, R120, R117

* - Default

m - Mount
nm - No Mount

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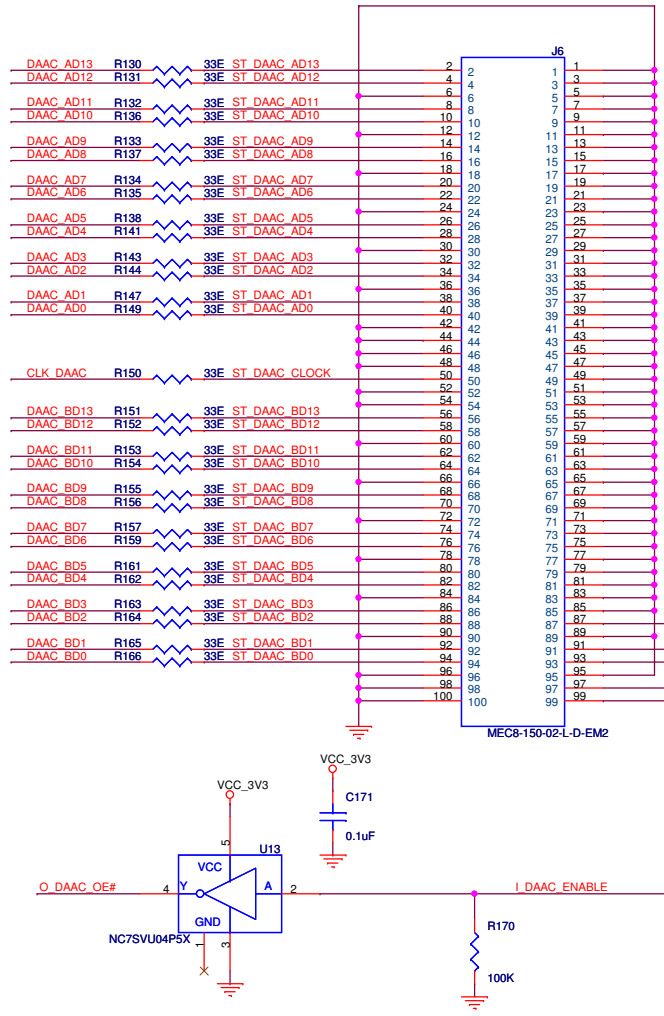
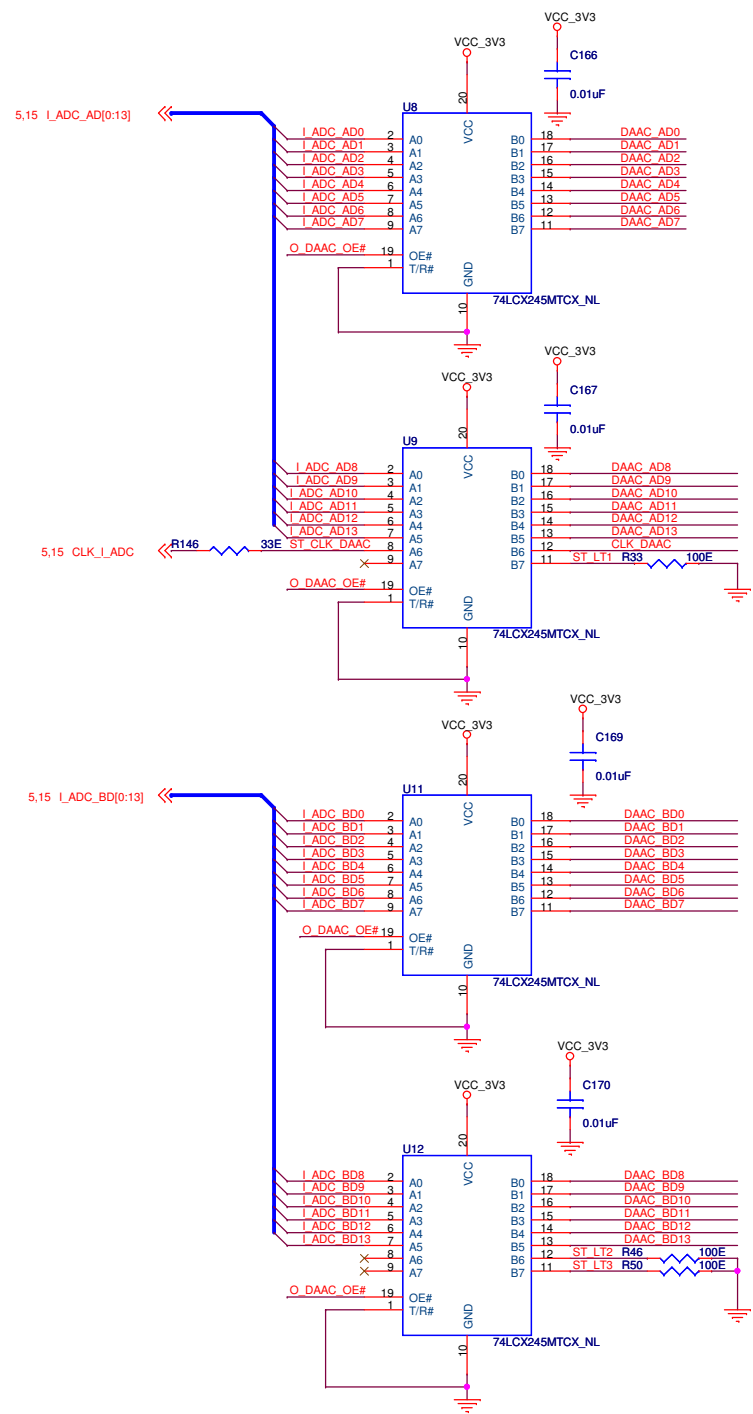
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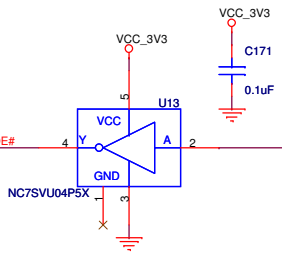
A/D CONVERTER

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FAST DAACs



Note : DC1098 is to be used as daughter card

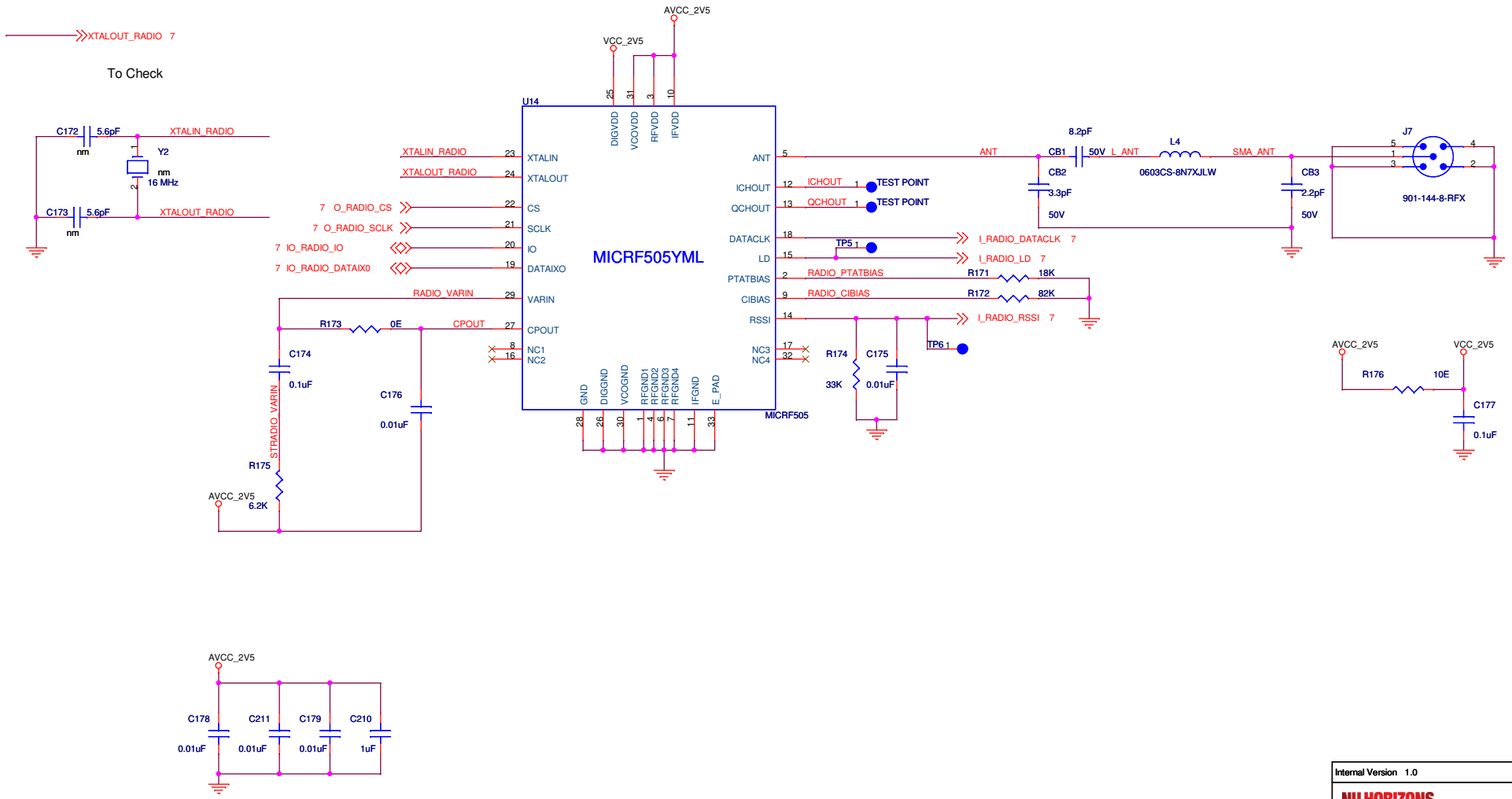


I_ENABLE_DAAC*	O_DAAC_OE#
0	1
1	0

*When the daughter card is inserted then I_ENABLE_DAAC becomes high

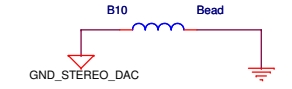
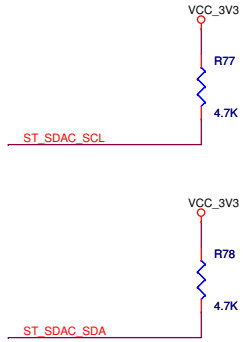
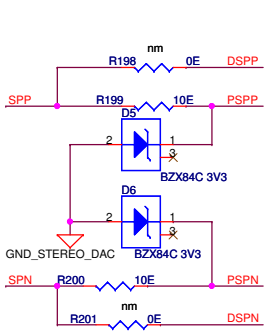
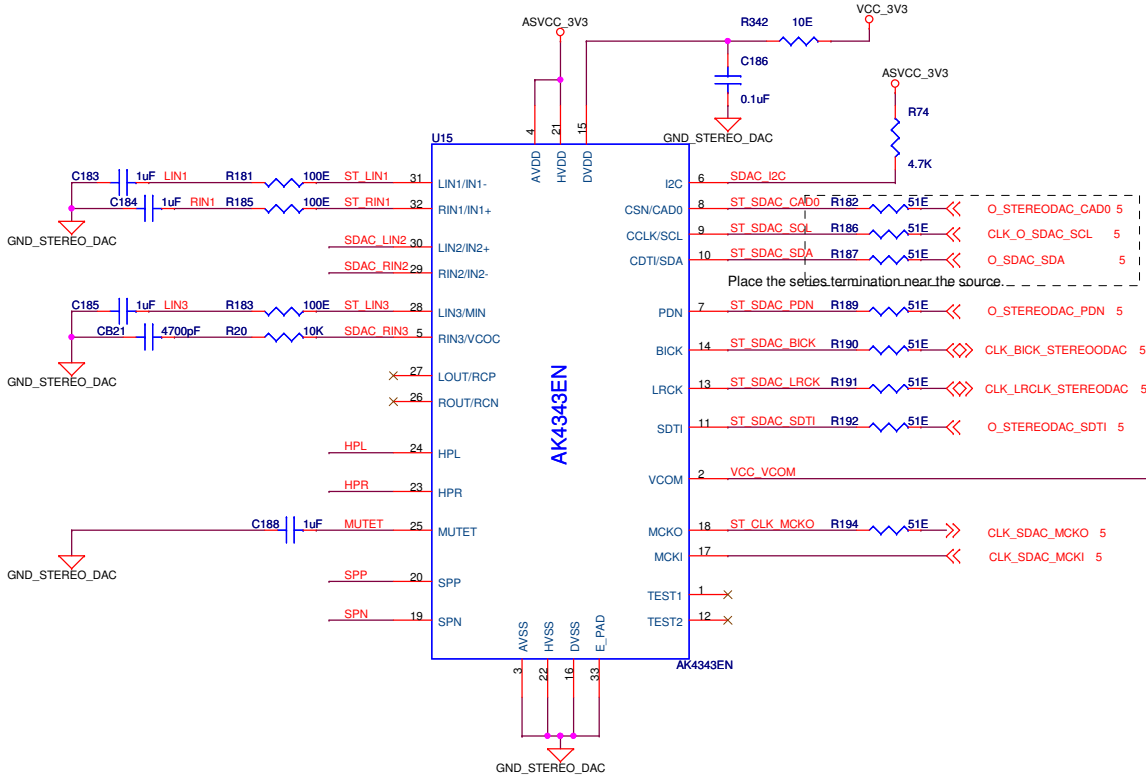
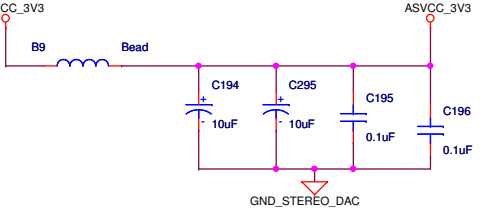
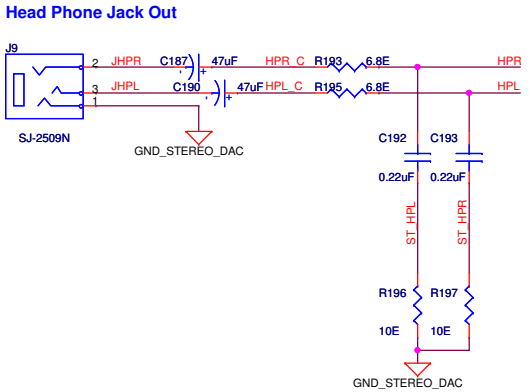
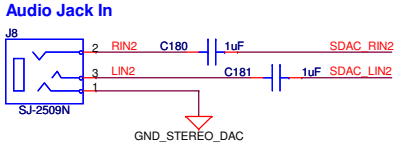
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RADIO TRANSCEIVER

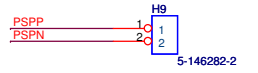
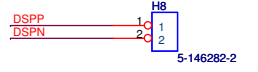
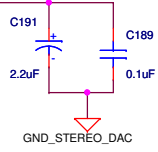
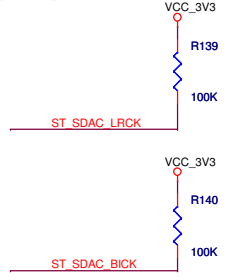
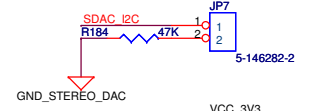


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RADIO TRANSCEIVER		
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STEREO DAC



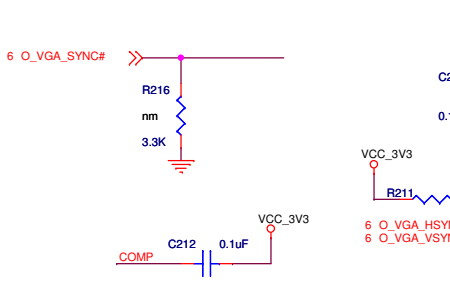
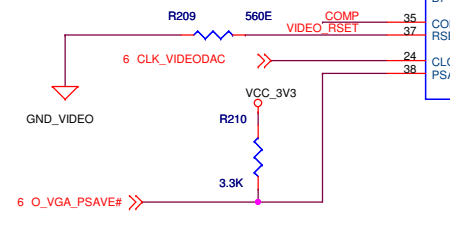
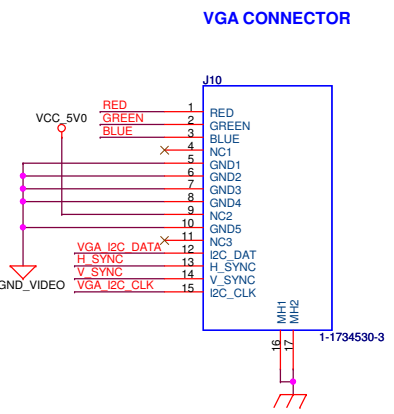
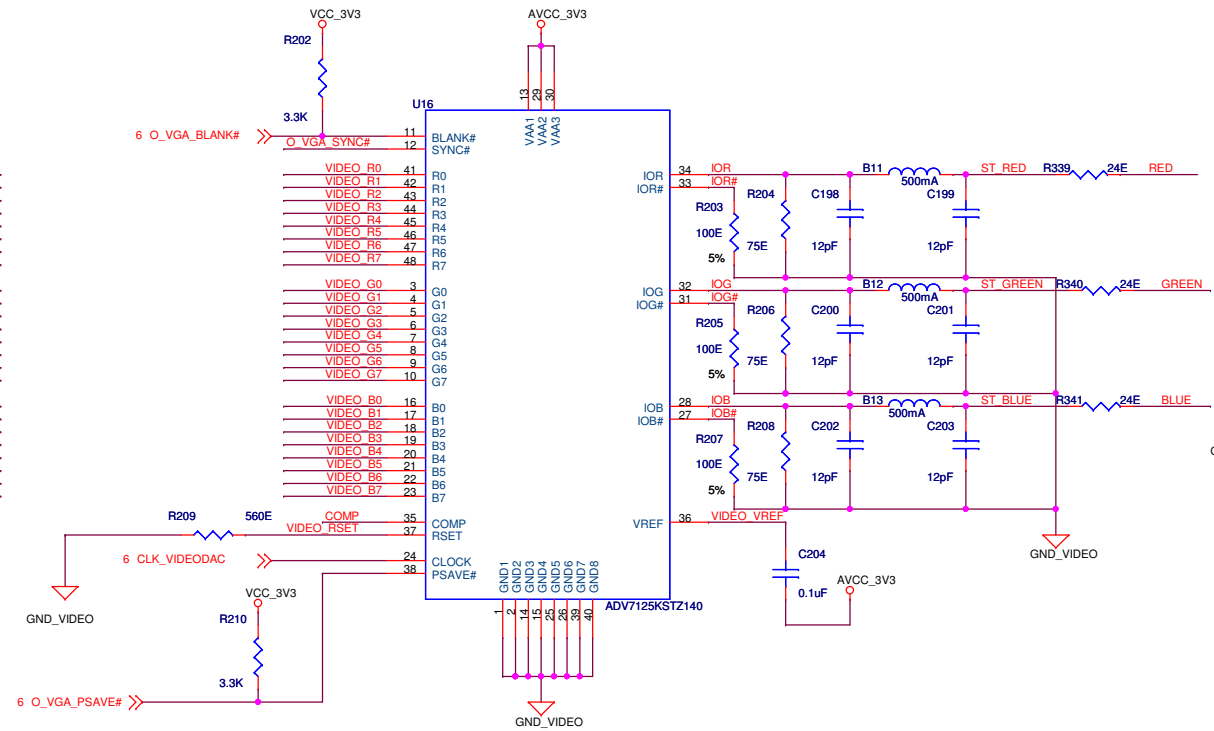
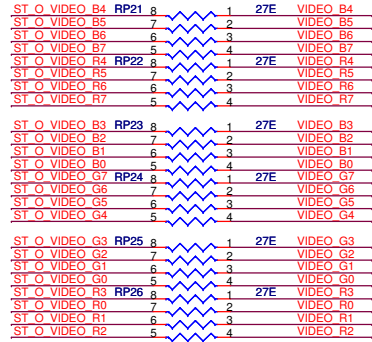
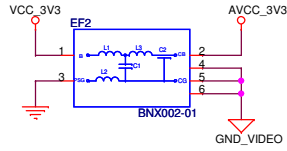
Mode Selection for I2C or 3-wire interface
Default : I2C Interface



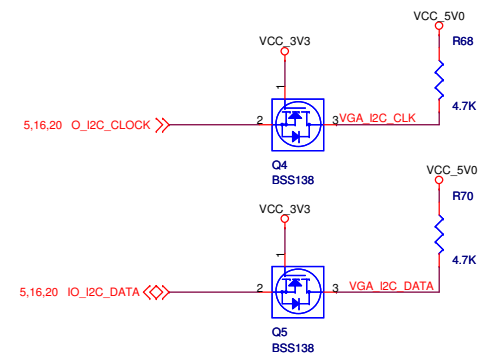
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6 ST_O_VIDEO_R[0:7] >>
 6 ST_O_VIDEO_G[0:7] >>
 6 ST_O_VIDEO_B[0:7] >>

VIDEO DAC



R276	HSYNCR, VSYNC Information
m	Not Required on Green Channel
nm	Required on Green Channel



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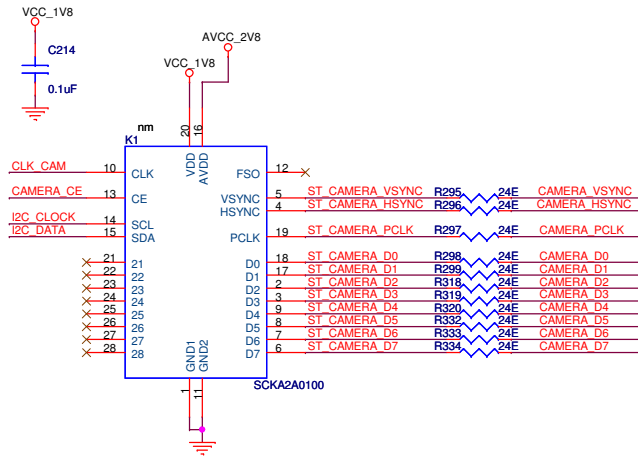
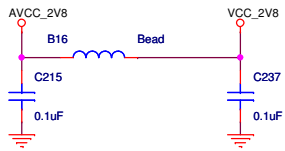
Tel: (631) 396-5000
 Fax: (631) 396-5050
 www.nuhorizons.com

Title: VIDEO DAC

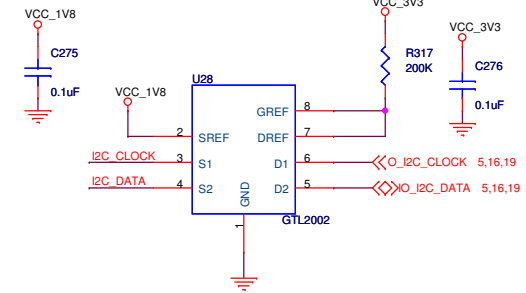
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CAMERA INTERFACE

→ L_CAMERA_D[0:7] 8

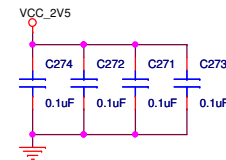
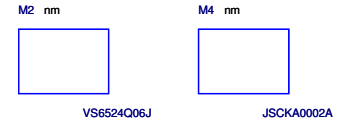
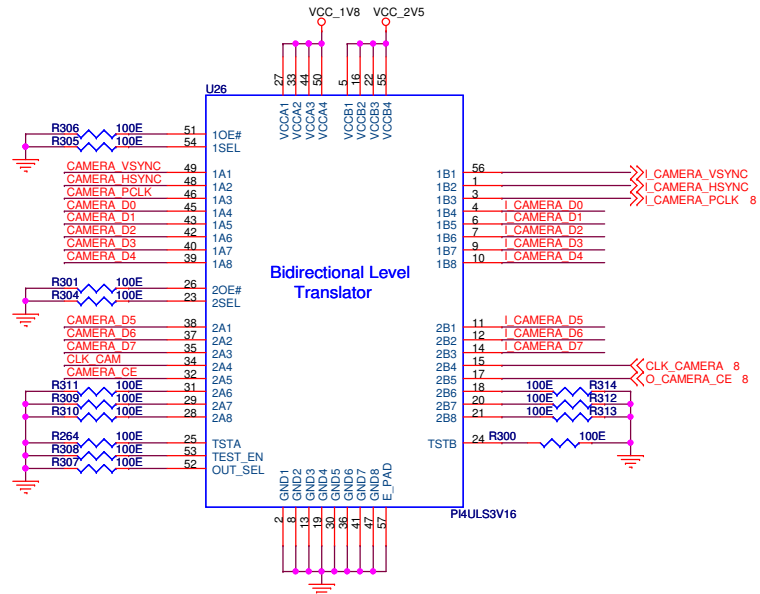
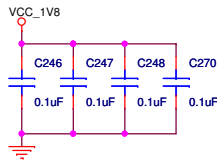


I2C LEVEL TRANSLATOR

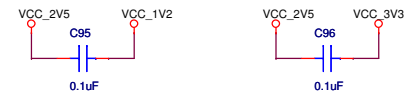


FPGA do not have 1.8V Bank. So level translators are used

LEVEL TRANSLATOR FOR CAMERA

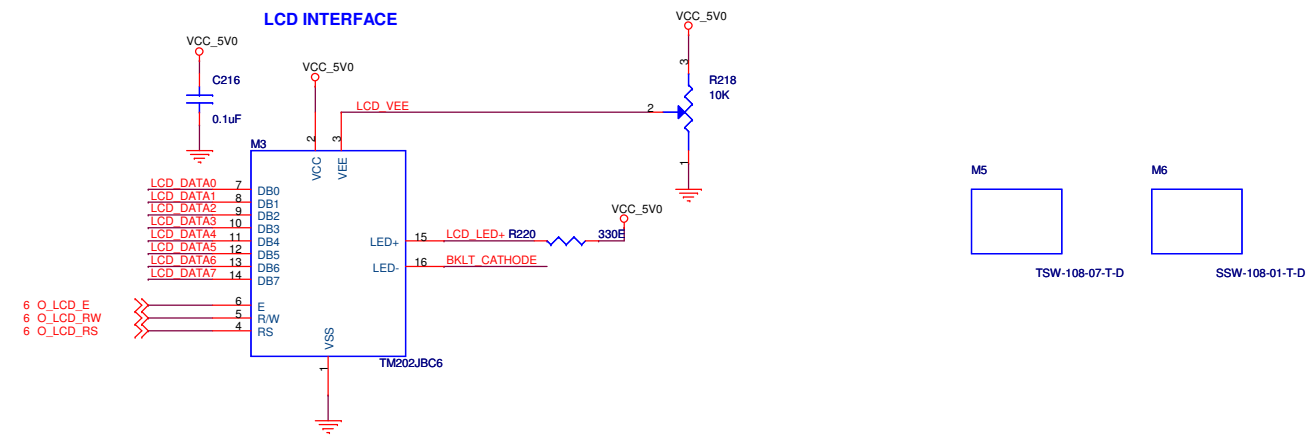


Stitching Caps

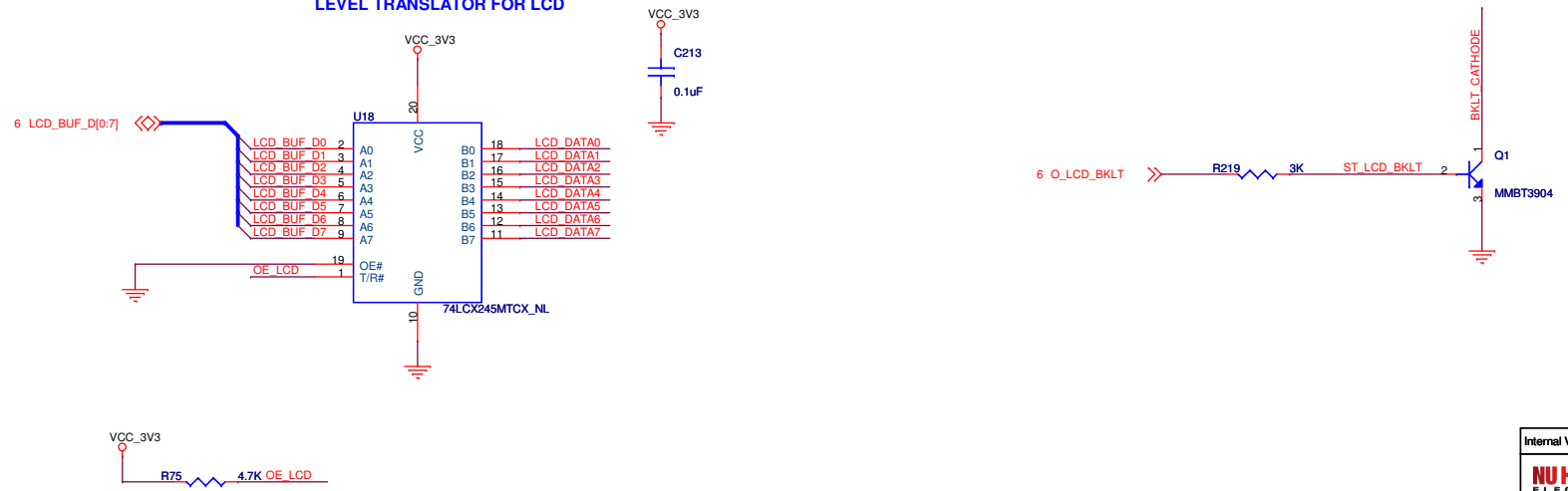


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LCD INTERFACE



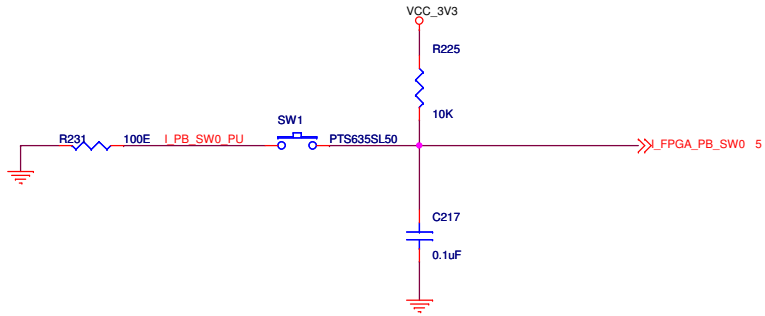
LEVEL TRANSLATOR FOR LCD



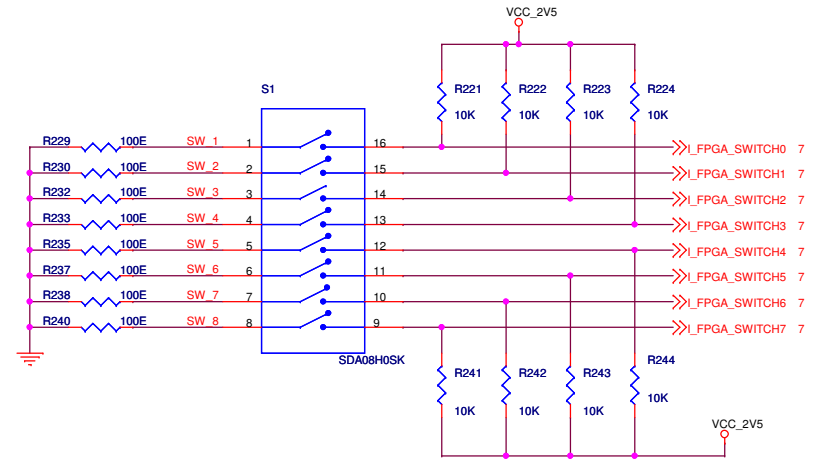
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Title LCD INTERFACE		
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LED DISPLAY & PUSH BUTTON

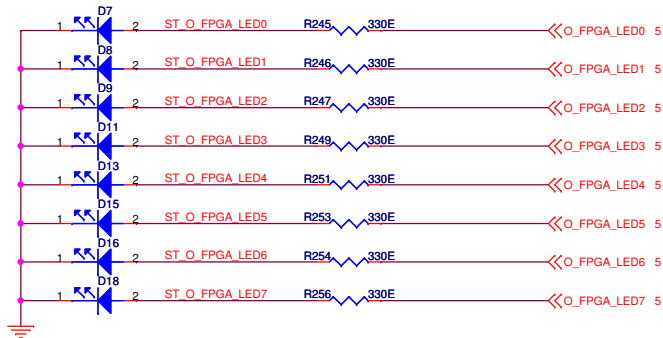
PUSH BUTTON



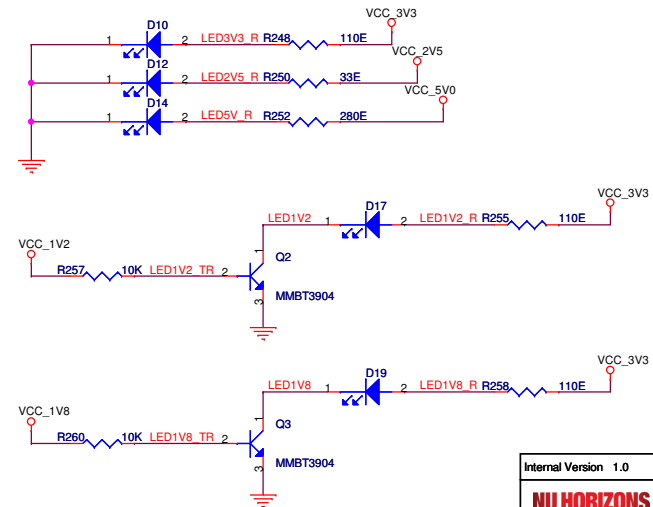
8 POSITION DIP SWITCH



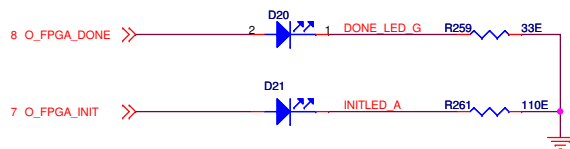
LED DISPLAY



POWER ON LEDS



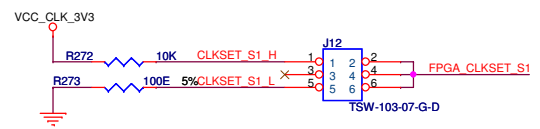
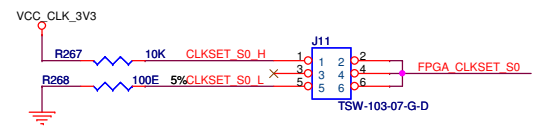
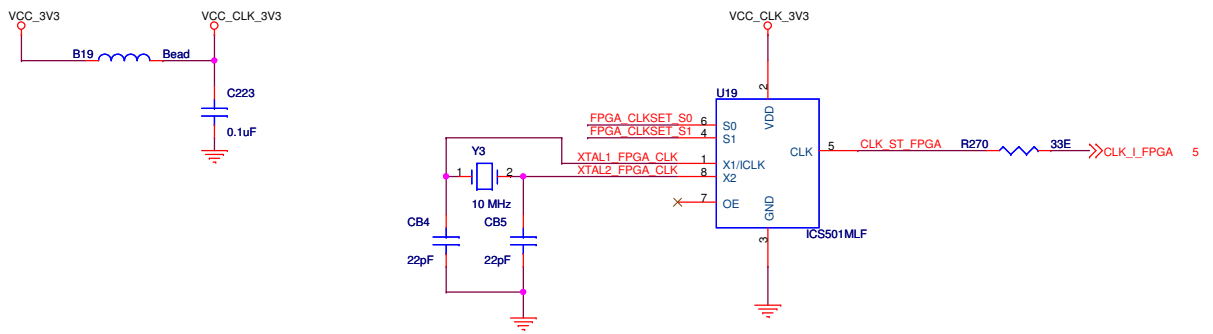
CONFIG STATUS LEDS



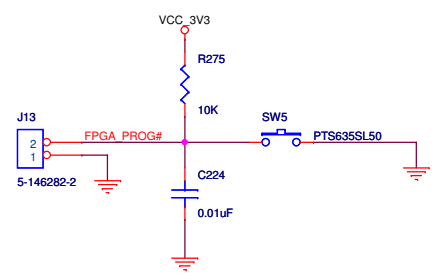
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Title LED DISPLAY AND PUSH BUTTON		
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CLOCK & RESET

FPGA_PROG# 8



FPGA RECONFIGURATION



Jumper should be inserted on J13 during SPI Flash programming using direct method

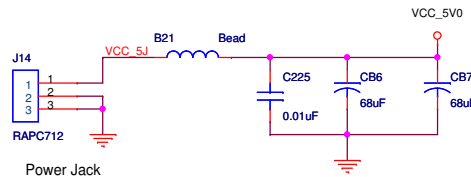
SN0	J12 (S1) (jumper setting)	J11(S0) (jumper setting)	Multiplying factor	O/P Frequency (MHz)
1	5 - 6 (L)	5 - 6 (L)	4	40
2	5 - 6 (L)	3 - 4 (M)	5.3125	53.125
3*	5 - 6 (L)	1 - 2 (H)	5	50
4	3 - 4 (M)	5 - 6 (L)	6.25	62.5
5	3 - 4 (M)	3 - 4 (M)	2	20
6	3 - 4 (M)	1 - 2 (H)	3.125	31.25
7	1 - 2 (H)	5 - 6 (L)	6	60
8	1 - 2 (H)	3 - 4 (M)	3	30
9	1 - 2 (H)	1 - 2 (H)	8	80

* - Default

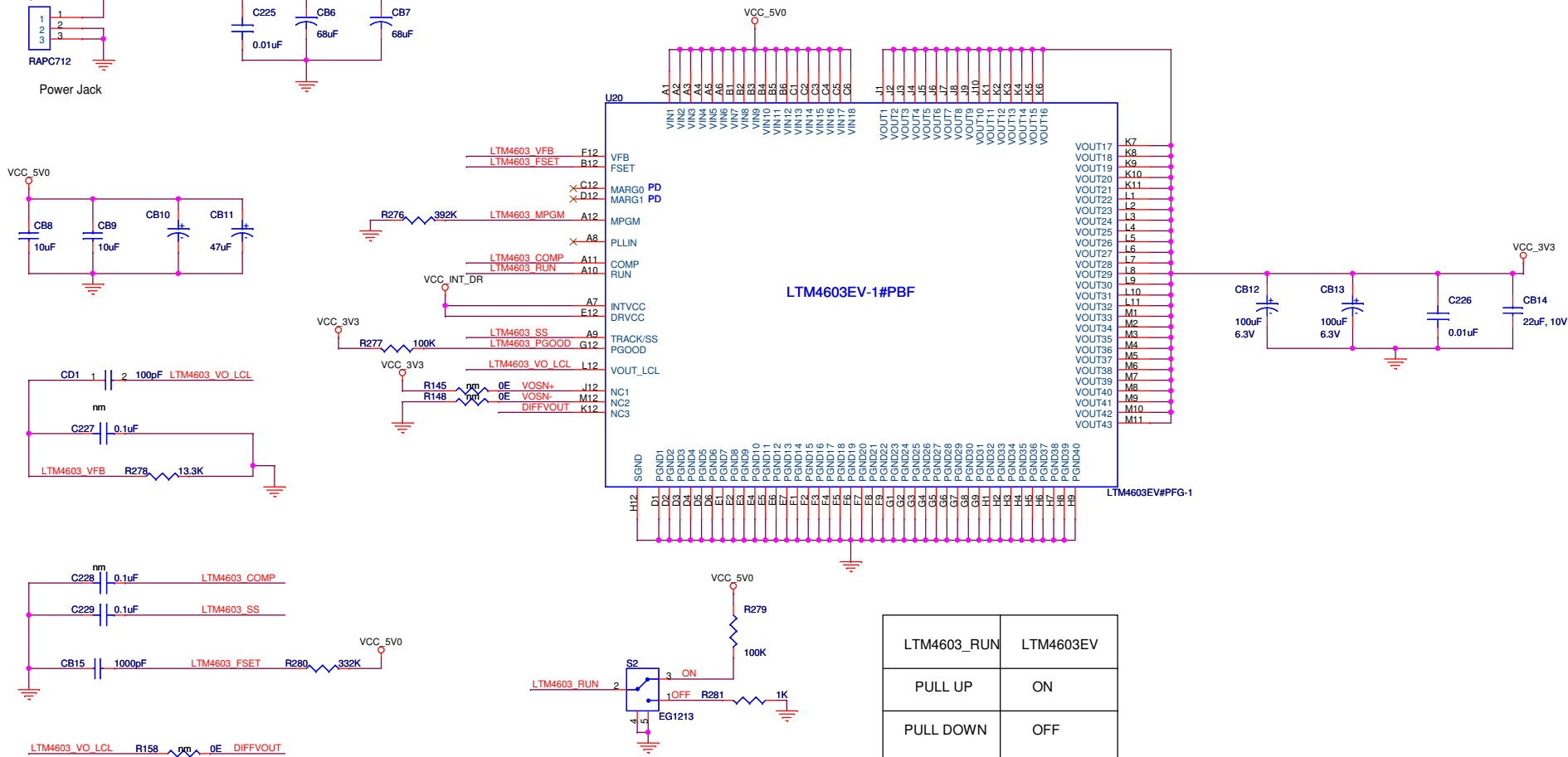
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Title: CLOCK & RESET		
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POWER_1

POWER JACK
5V @ 5A



SWITCHING REGULATOR
3.3V @ 6A FROM 5V



LTM4603_RUN	LTM4603EV
PULL UP	ON
PULL DOWN	OFF

Internal Version 1.0

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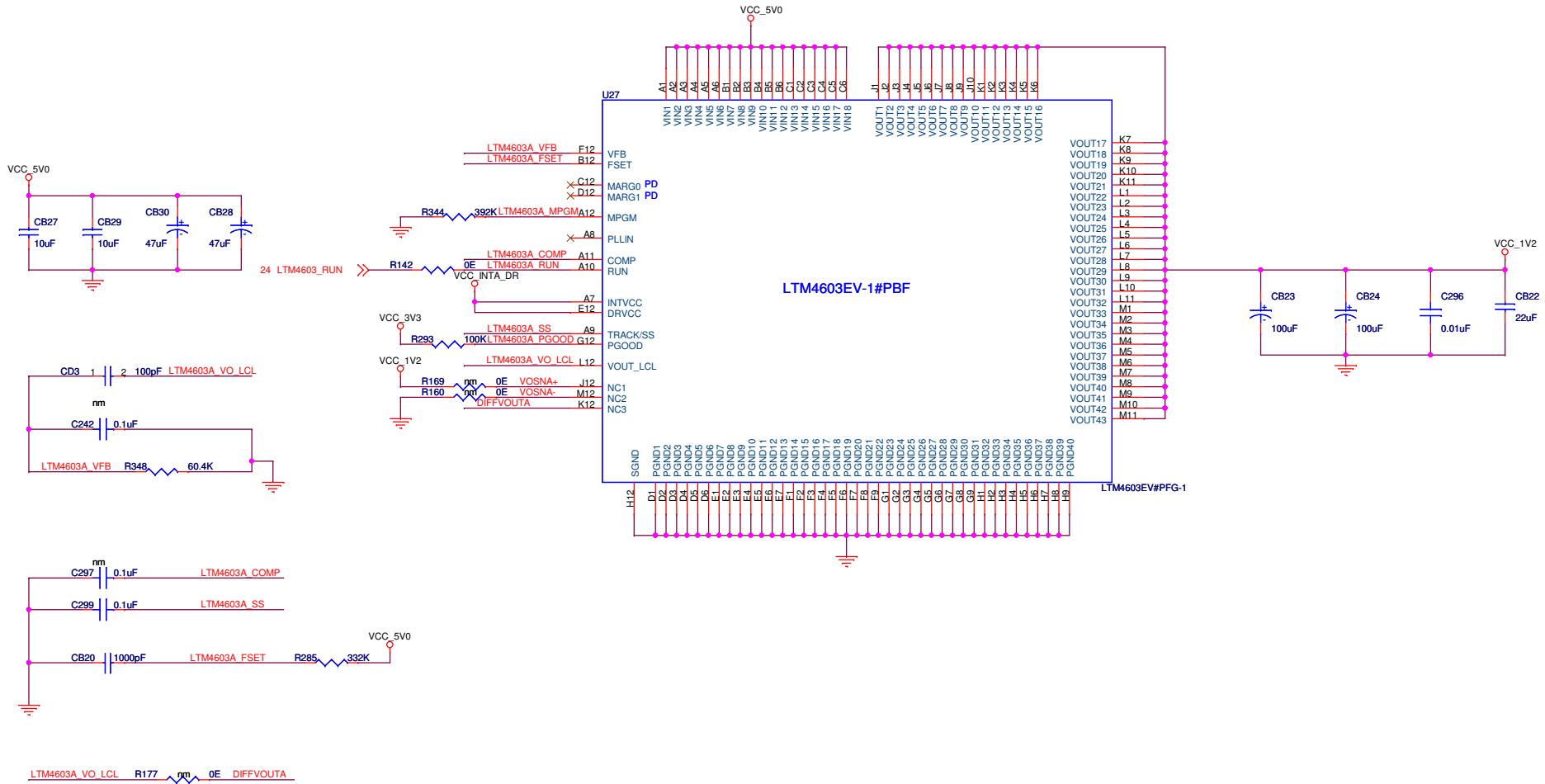
Title: POWER_1

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POWER_2

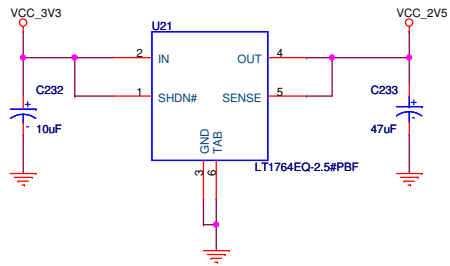
SWITCHING REGULATOR
1.2V @ 6A FROM 5V



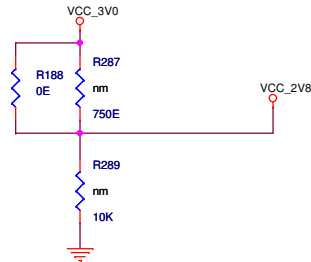
Internal Version 1.0		
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Title: POWER_2		
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POWER_3

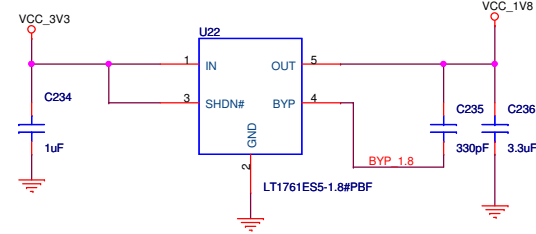
LDO
2.5 V@3A From 3.3V



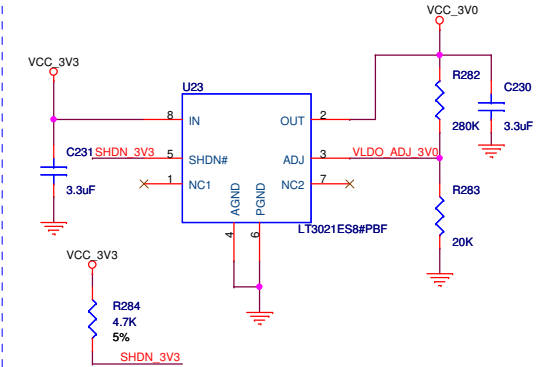
TO CAMERA
2.8V @ 9mA From 3V



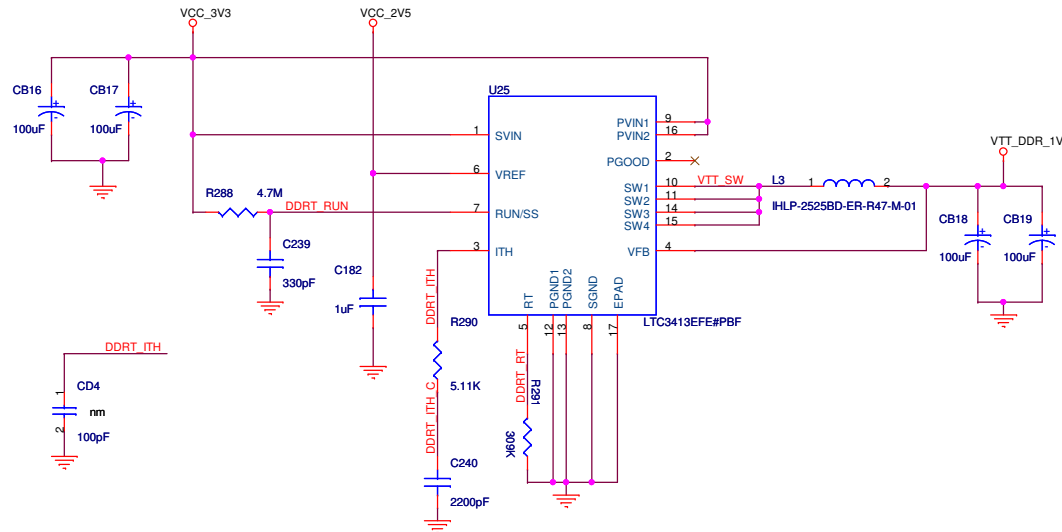
LDO
1.8 V@100mA From 3.3V



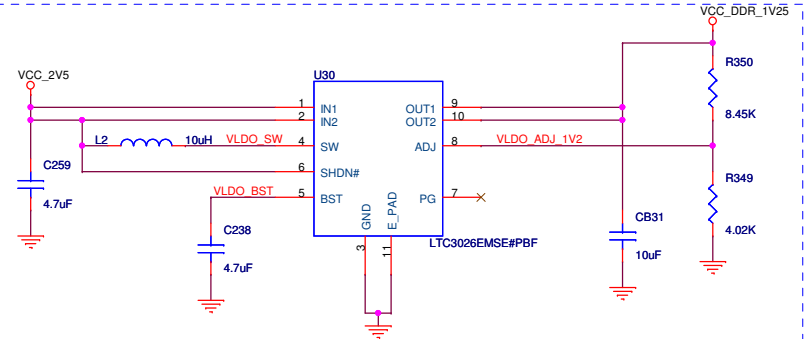
VLDO
3V@ 500mA From 3.3V



DDR TERMINATION REGULATOR
1.25V @3A From 2.5V



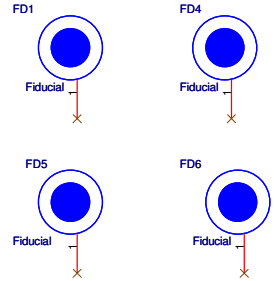
VLDO
1.25V @ 1.5A From 2.5V for DDR Vref in FPGA



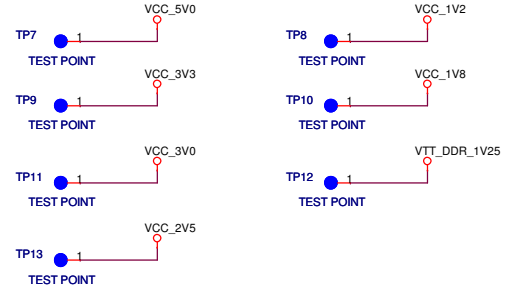
Internal Version 1.0		
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Title POWER_3		
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BOARD ACCESSORIES

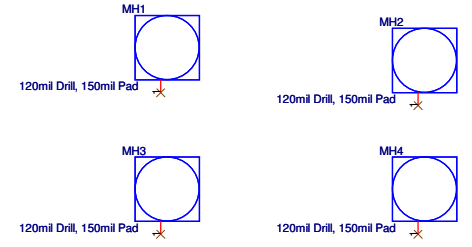
GLOBAL FIDUCIALS



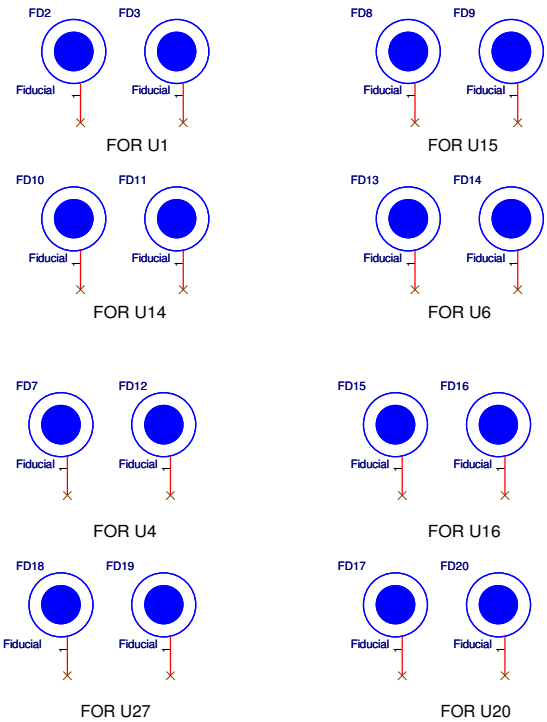
TEST POINTS



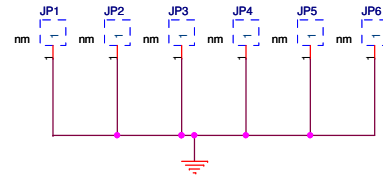
MOUNTING HOLE



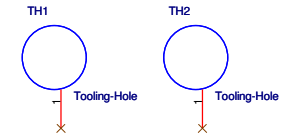
LOCAL FIDUCIALS



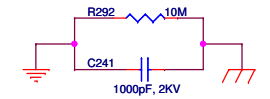
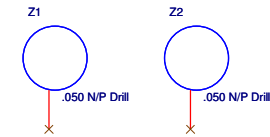
GROUND POSTS



TOOLING HOLE



REWORK HOLE



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REVISION HISTORY

REV	VER	DATE	NOTES
A	0.1	02/07/2007	Added Power Scheme
	0.2	24/07/2007	Power Scheme is modified. Block diagram is updated and All the interfaces have been done.
	0.3	20/08/2007	Test point is added for 3.3V Radio chip power supply is changed to 2.5 V In RJ45 Connector, Transformer T2 pin no.5 is pulled up to 3.3.V Ethernet: crystal is no mounted, video dac 50 MHz Oscillator is no mounted ADC OVDD is connected to 3V Balun transformer is added in ADC Two on chip DDR are added
	0.4	22/08/2007	KSZ800L is changed to KSZ8041NL
	0.5	07/09/2007	DDR Swaplist were done DDR series termination resistor for clock is added RS232 5th Pin is connected to circuit ground Stereo DAC: Exposed PAD is connected to analog ground plane RJ45 termination is connected to ground through 0.1uF DDR Termination regulator input voltage is changed to 3.3V Fast DAACs feedbacks are implemented ADC ground is connected to digital ground
	0.6	05/12/2007	VGA I2C Signals are added and optional 5V pin is connected to 5V AKM Feedback:10uF is added JTAG Header voltage and configuration pin pull up resistors been pulled up to 3.3V instead of 2.5V Two pairs of local fudicials are added.video dac pull up resistors are changed to vcc_3V3 Power Section is modified Radio SCLK net was changed
B	0.1	09/04/2008	LCD Interface: Pull up resistor is added at the level translator No. of DDR SDRAM changed to one DDR Vref is given DDR and Radio Section are completely modified Stereo DAC : Pull up resistors to I2C signals are added SPI Flash supply voltage is changed to 3V No. of push button is changed to one Camera module analog supply voltage is changed to 3V Radio : Frequency is given from the FPGA

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