NU HORIZONS ELECTRONICS

Spartan 3A DSP Reference Kit User Manual

Customer/Partner	Nu Horizons Electronics Corp
Version	VA101
Date	May 29, 2008

Revision Log

Revision	Date	Description
VA001	Jan 29 , 2008	Initial Release
VA100	May 28 , 2008	Updated the GUI for FPGA Configuration
VA101	May 29 , 2008	Updated the GUI for ISE10.1

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1. Introduction

This User Manual describes the Nu Horizons Spartan-3A DSP Reference Kit, the NH-SPAR3ADSP-EVL

1.1. Scope and Purpose

This document describes the hardware design specifications of Spartan-3A DSP reference kit.

This document serves as the design specification, and describes the hardware implementation details (electrical and mechanical) pertaining to this board.

1.2. How to use this document

This document describes the features and interfaces of the Spartan-3A DSP Reference Kit. This book contains the following sections:

- Overview provides a brief overview of the FPGA. Some chip aspects important to understanding the board design are also discussed in detail.
- Getting started provides brief notes on unpacking the board, cabling, interconnections, module connections and power up guidelines.
- Board Design describes the architecture of Spartan-3A DSP Reference kit.
- Configuration describes the various methods used to configure Spartan 3A DSP FPGA.
- Displays section describes all LED Indication and LCD on the board.
- DIP switch & Push button describes the function of all switches on the board and their default settings.
- Signal Notations:

Signal	Notation
Active Low Signals	#
Logical High for voltage levels	1
Logical Low for voltage levels	0

Table 2: Signal Notations

2. Overview

The Spartan 3A DSP reference kit is an integrated circuit development platform for Xilinx's Spartan 3A DSP FPGA. The reference board is based on Xilinx's newest programmable architecture and contains 189Kbytes of block RAM, Digital clock management, multiboot reconfiguration, design authentication using device DNA configuration and flexible I/O's. The reference board also features external non volatile memory (SPI flash) and volatile (DDR SDRAM) memory, power supplies, LCD ports, Audio, Camera, Video Interfaces and other I/O devices.

The Spartan-3A DSP Reference Kit provides a platform for engineers for designing highly integrated designs made possible with Xilinx Spartan-3 FPGA family. This document provides the basic information on Spartan 3A DSP reference board capabilities, functionalities and design. The board provides the necessary hardware to evaluate the features of the Spartan-3A DSP and to implement complete user applications.

This document lists and explains the features of the board, the system level block diagram with all major components identified for the design, and the interfaces. The various subsystems are explained separately. This document also lists connectors and signal distributions across the board.

The power for the board is generated from a 5V external power jack.

The form factor of this board is 6 x 4 inch. The Spartan-3A DSP FPGA used in this reference board is XC3SD1800A, which consists of 1800K logic gates and 519 maximum users IO's.

3. Board Features

FPGA

- Xilinx XC3SD1800A Spartan 3A DSP FPGA in the 484 ball BGA Package (CS484)

Memory

- 16 MB SPI Flash from ST Microelectronics
- 32 MB on Board DDR SDRAM from Micron

Interfaces

- RS232 serial port with LT1331CG transceiver
- 10/100 Ethernet PHY KSZ8041
- Analog to Digital Converter LTC2285
- Radio Transceiver MICRF505YML
- Stereo DAC AK4343EN
- Video DAC ADV7125
- Camera Module VS6524
- 20x2 character LCD Display TM202JBC6

Power

- Power Jack (5V @ 5A AC to DC Adapter)

FPGA Configuration Options

- SPI Serial Flash
- JTAG

Buttons and Switches

- 8 position DIP switch
- 8 Discrete LED's
- One push button Switch
- Push Button Switch to initiate FPGA programming.

Connectors and Features

- Fast DAACs Connector MEC8-150-02-L-D-EM2
- Complete RoHS compliant development solution
- Includes board, quick-start guide, Wall Adapter
- Cables are not included and must be ordered separately
- Evaluation software and example codes are in the website http://www.nuhorizons.com/xilinx/boards/spartan3a/DSP_Eval_kit/

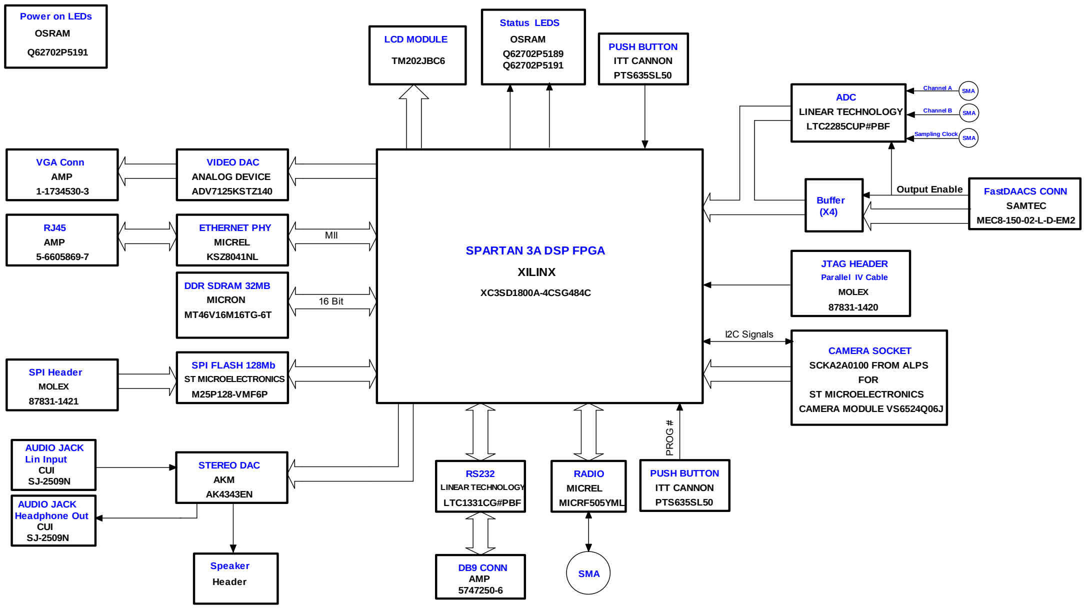

Figure 1: Board Block Diagram

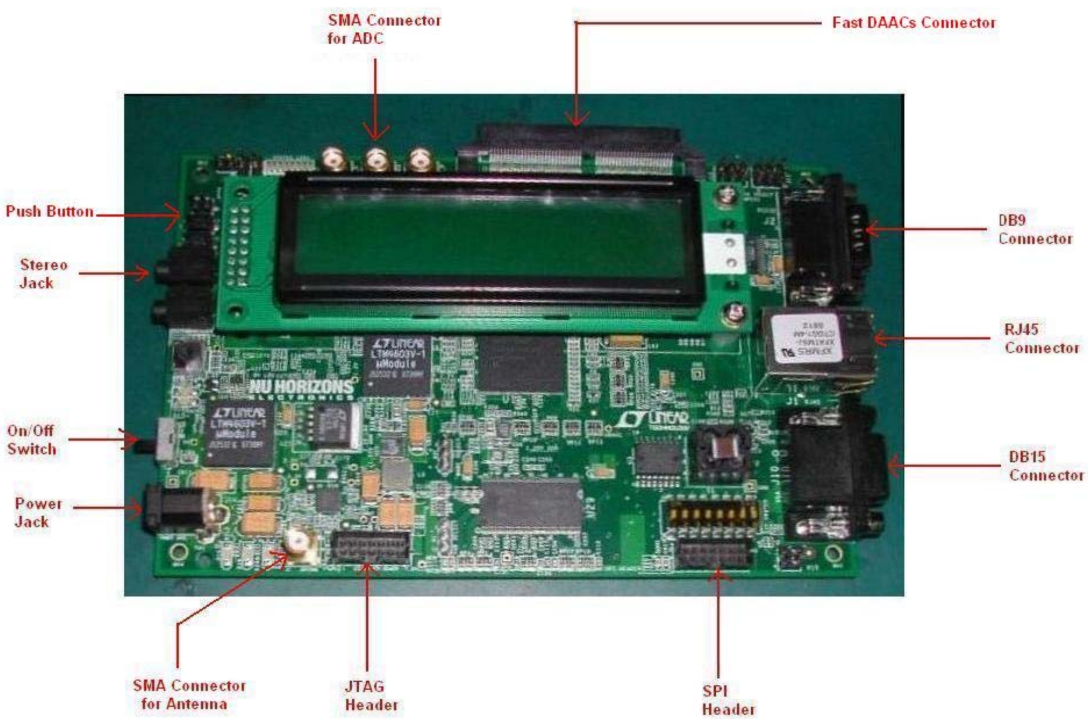

Figure 2: Assembled Board Photo (Top View)

3.1. Electrical Specifications

The Spartan-3A DSP Reference Kit is powered from an external 5V AC/DC Adapter (supplied with the kit).

Supply Voltages 5Volt:

The 5Volts to the board is supplied through the power jack. The 5Volts should be within the tolerance of +/- 5 %. The maximum ripple should be less than 144mV. 5Volts is main power source for the board. All the other voltages are derived from 5V supply only.

- AC/DC adapter is provided with the kit. To power the board with an external supply, the user should provide +5V to a standard 2.5mm barrel connector (J4). Note that the connection to the barrel connector has center positive.

Voltage (V)	Current drawn (mA)	Maximum Power Drawn (mW)
5	132.6	663
3.3	659	2174.7
3	575	1725
2.5	527.5	1318.75
1.8	47.6	85.68
1.25	926	1157.5
1.2	3848	4617.6

Table 3: Electrical Specifications

WARNING: Do not operate beyond the rated voltages this may cause permanent damage to the board.

3.2. Environmental Specifications

PRECAUTION: Do not ship or store near strong electrostatic, electromagnetic, magnetic or radio active fields.

3.3. Mechanical Specifications

Spartan 3A DSP Reference Kit is designed with the form factor of 6” x 4”

3.4. Design Tool

- Xilinx ISE 10.1i Web pack

4. Getting Started

4.1. Unpacking

Check the shipping carton for any damages. If the shipping carton or contents are damaged, notify the carrier and supplier. Retain the shipping carton and packing material for inspection by the carrier. Save the anti-static bag for storing or returning the board.

Verify the contents of package with the shipping documents. Please inform the supplier for any discrepancies.

Standard Items:

- One Spartan 3A DSP Reference Kit
- Universal AC to DC Adapter
- Product Flyer

4.2. ESD Requirement

While handling the board, make sure the lab bench and the operator are connected to ESD Strip.

Caution: Use ESD Strip while handling the board.

4.3. Interconnections/Cabling/Modules

- Connect the COM Port 1 of the PC to the DB9 serial Port connector (J2) through a null modem cable.
- Connect the Parallel IV Cable to the JTAG header (H3) for configuration using JTAG mode or connect the Parallel IV Cable to SPI header (H4) for configuration using direct SPI mode.
- Connect the 5V adaptor to the power jack(J14) in the board
- Connect the VGA connector J10 to the monitor via the DB15 Cable.
- Connect the RJ45 Connector cable of the PC to the RJ45 Connector J1.
- Input to the Analog to Digital converter is given through SMA Connector J3 and J4. Clock is given through J5.

4.4. Powering-up

- Connect the 5V power adapter to the power jack (J4).
- The LED D14 will glow and switch on S2.
- Verify the voltage level at the following test points detailed in **Table 4**. Verify the voltage rails for the correct voltages: Only one rail should be checked at a time. Before powering up, set up the voltmeter and have the probes in place. Then, power-up the board, check the voltage of this rail and power-down the board immediately. This method should be repeated for each and every voltage rail.

Voltage Level	Test Points
5V	TP7
3.3V	TP9
3V	TP11
2.5V	TP13
1.8V	TP10
1.25V	TP12
1.2V	TP8
1.25 V	CB31.1

Table 4: Voltage Test Pads

4.5. FPGA Initialization and configuration

- During power up or when SW5 is pressed (PROG_B pin goes low), the Spartan 3A DSP FPGA goes through the initialization sequence to clear the internal FPGA configuration memory. At the beginning of the sequence, both the DONE pin and INIT_B pin of FPGA goes low. When initialization is complete, the INIT_B pin goes HIGH. As soon as INIT _B goes high the RED LED glows.
- When initialization is complete, the FPGA is ready to be configured. By default, the FPGA is configured in JTAG mode.
- Program the given BIT file using the JTAG header (H3).
- The bit file is converted into .mcs file and it is loaded into the SPI Flash by direct or indirect method of SPI Programming using SPI header H4 which is the best method of configuring the FPGA. For further details refer **Section 7.2**

5. Board Design

5.1. Spartan-3A DSP FPGA

The Spartan XC3SD1800A-4CSG484C is the device selected for this Spartan 3A DSP Reference kit. The XC3SD1800A consists of 1800K logic gates and 519 maximum users IO's.

Features

- Low cost and high performance logic solution.
- Suspend and Hibernate modes reduce system power.
- Configuration interface to industry standard Low cost Space saving SPI serial Flash PROM.
- Complete ISE 9.2i and web pack development system support
- Micro blaze and Pico blaze embedded processor core
- Low cost BGA Packaging & Pb free option.
- Multiboot reconfiguration
- Design Authentication using Device DNA
- Configuration CRC Checker

The footprint of FPGA is CS484, Fine pitch thin BGA package with a ball pitch of 0.8 mm in 19 X 19mm package.

Spartan 3A Part	System Gate	Logic Cells	Block RAM (Bits)	DSP48As	DCM's	Maximum User IO's	Maximum Differential IO Pairs
XC3SD1800A	1800K	37,440	1512K	84	8	519	227

Table 5: Spartan 3A DSP FPGA Attributes

5.2. Configuration

Spartan 3A DSP Reference Kit supports Boundary scan (JTAG) and SPI programming methods of configuration The configuration mode can be changed using the Mode pins (M0, M1, and M2) on the FPGA. Two options to configure FPGA are described below.

- Programming on board 16MB SPI serial Flash, then programming the FPGA from the image stored in the SPI Flash using SPI serial mode.
- Download the FPGA design directly to Spartan 3A FPGA by using JTAG interface

Configuration Mode	M2 (H2) pin	M1	M0
JTAG*	1(2-3)	0	1
SPI	0 (2-1)	0	1

*Default

Table 6: Configuration Mode for FPGA

5.2.1. Master SPI Mode: SPI Flash Programming

In SPI Serial Flash mode (M [2:0] = <0:0:1>), the Spartan-3A DSP FPGA is configured from SPI Serial Flash memory. In this mode, the FPGA supplies the CCLK output clock from its internal oscillator to the clock input of the attached STMicroelectronics SPI Flash device. The Variant select pins are used to select the read mode of FPGA.

To configure FPGA in SPI mode a 2 pin link jumper should be installed on H2 as described in **Table 6** in such a way to make M[2:0]=001.
There are three primary methods of programming SPI flash memory as described below

- Third party programmer
- Indirect in-system programming
- Direct in-system programming

5.2.1.1. Third Party Programming

SPI memory can be programmed off-board using a third party SPI programmer. This method is advantageous for mass production.

5.2.1.2. Indirect in-system programming

The SPI memory can be programmed via JTAG chain of the FPGA. The FPGA has JTAG test capabilities, which include the standard commands. When using these commands, it is possible to drive and sample the pins of the FPGA with the JTAG chain and thereby stimulate the pins of the SPI memory via the traces routed on the PCB. Figure 6 shows the JTAG chain connected to SPI flash.

The advantage to this approach is that it requires minimal wiring for in-system programming. The disadvantages include relatively slow SPI programming speed and the requirement for a third party JTAG programmer, which supports that particular SPI device used.

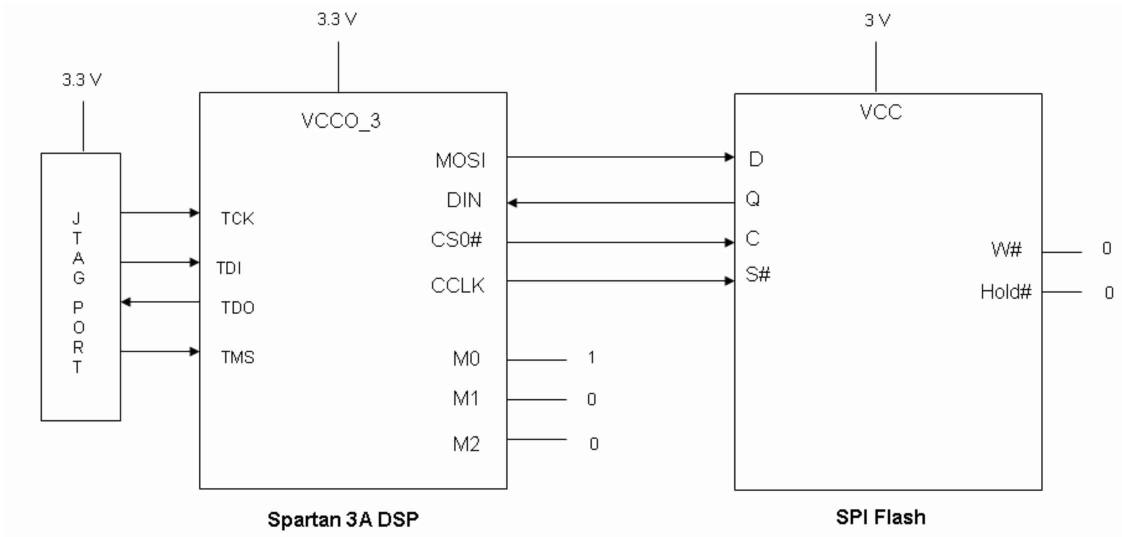

Figure 3: Indirect In-system SPI Programming

5.2.1.3. Direct in-system programming

For direct in-system programming Xilinx has a software utility called XSPI that can be used to program a limited set of SPI flash memories. Using a Xilinx parallel cable and host computer, the XSPI utility programs the SPI Flash memory device directly in-system.

For direct in-system programming with the XSPI utility, ensure that the FPGA pins driving the MOSI, MISO, SCLK, and SS_n signals are in all high- impedance state. There are three methods to place these signals in High impedance state as follows:

- Holding the FPGA's PROG_B pin Low using the push button SW5 or insert the link jumper in J13, so that all the IO pins are in the tristate. The FPGA is unconfigured during the programming process and automatically loads the new SPI Flash PROM image when PROG_B is released high.
- Alternately, changing the FPGA's mode pins to JTAG mode (M [2:0] = <1:0:1>) and pulse PROG_B pin in the forces all the FPGA I/Os to high-impedance. The FPGA is unconfigured during the programming process. The FPGA’s mode pins should be changed to SPI mode (M [2:0] = 0:0:1) and PROG_B must be pulsed low before the FPGA reloads the SPI Flash PROM image.
- Within the functioning FPGA application use an internal control signal that tristate the SPI Flash pins. The FPGA remains configured with the current configuration. Pulse the PROG_B pin low and issue a multiboot reconfiguration operation with a start address of zero.

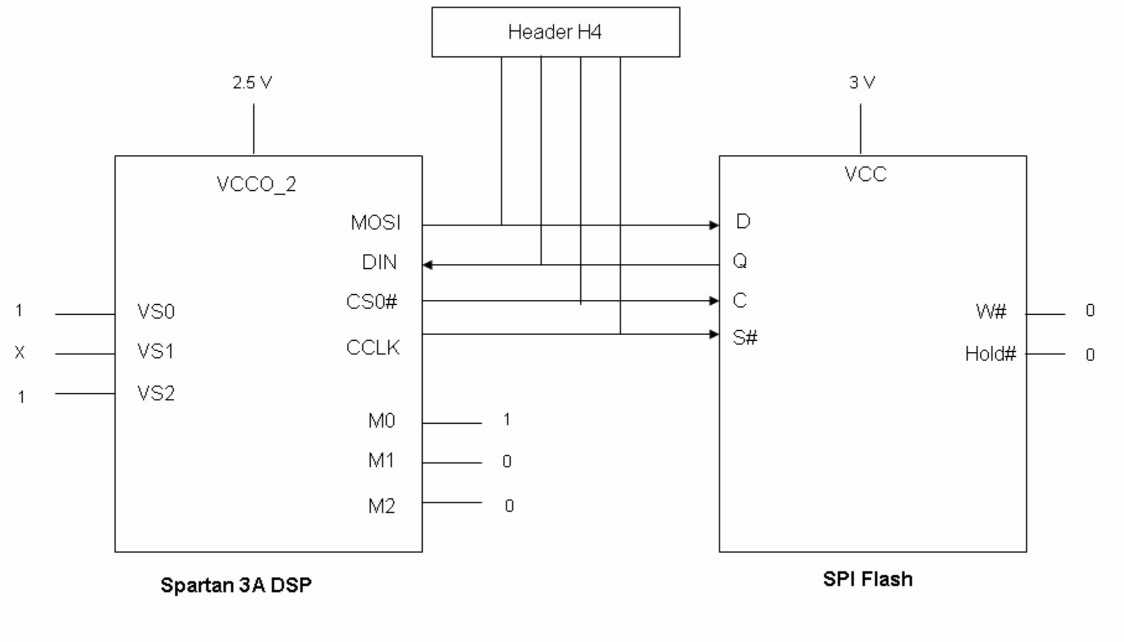

Figure 4: Direct In-system SPI Programming

For further information regarding XSPI utility, please refer Xilinx Xapp445, http://www.xilinx.com/support/documentation/application_notes/xapp951.pdf

In SPI mode, the FPGA samples the Variant Select (VS [2:0]) pins to determine which SPI command sequence to issue. VS0 and VS2 of the variant select pins are fixed, and only VS1 (H1) will decide the sequence of the command issue (Fast read or Normal read) .The following table describes the jumper setting of command sequence.

Jumper setting (H1)	SPI Command	VS0	VS1	VS2
1-2	FAST READ (0x0B)	1	1	1
3-2	READ (0x03)	1	0	1

Table 7: Variant Select Jumper setting

5.2.2. Boundary Scan JTAG

A JTAG parallel IV cable (not included in the kit) is required to program the Spartan-3A DSP FPGA via Boundary-scan. When programming the FPGA via the JTAG interface, Mode pin M [2:0] is set to 101. Note that power should be removed when changing the programming Mode. The parallel IV JTAG pin outs are as follows.

JTAG Pin No.(H2)	Net Name	FPGA Ball No.
2	3.3 V	
4	TMS	B1
6	TCK	A21
8	TDO	B22
10	TDI	D2
(1,3,5,7,9,11,13)	GND	

Table 8 : Parallel IV JTAG Header to FPGA Pin outs

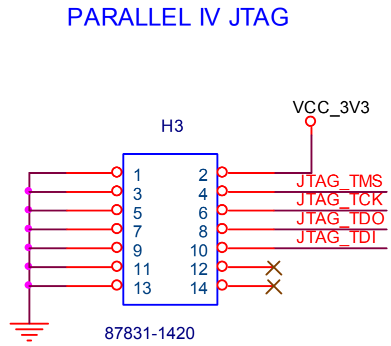

Figure 5: Parallel IV JTAG Header

5.3. Memory

The Spartan-3A DSP reference kit is populated with a 128Mbit low voltage serial flash memory from ST Microelectronics and one 32 MB onboard DDR SDRAM. SPI Flash memory may be used to configure the Spartan 3A FPGA or to store user data and processor soft core (Micro blaze or Pico blaze).

5.3.1. SPI Flash

The 128M bit SPI Flash (M25P128VMF6P) from ST Microelectronics is used to store configuration data for Spartan-3A DSP FPGA.

Features of Serial Flash memory are:

- Able to migrate from lower density to higher density with the same footprint
- Up to 50MHz SPI bus serial interface
- 2.7V to 3.6V single supply voltage operation
- Deep power down mode
- Bulk Erase (16Mbit) in 13s

Since the FPGA programming pins are available to the user after configuration, it is possible to use memory for external data storage. The following table illustrates the pin-outs of the FPGA to SPI flash memory.

SPI Flash PIN No.	SPI Flash Pin Name	Signal Name	FPGA Ball No.
1	HOLD#	-	-
7	S#	CSO#	U7
9	W#	-	-
8	Q	MISO	W17
15	D	MOSI	V13
16	C	CONFIG	V17

Table 9: SPI Flash to FPGA Pin outs

5.3.2. DDR SDRAM Interface

This board has on board DDR in TSSOP package (MT46V16M16TG-6T from Micron) has16 bit data bus that supports up to 32 MB. The DDR clock is 167MHz and it is given from FPGA.

Name	Net Name	FPGA Ball No.
IO23_L12P_2/D7	WE#	AB10
IO24_L12N_2/D6	CAS#	AA10
IO25_L13P_2	RAS#	Y8
IO26_L13N_2	CS#	Y9
IO27_L14P_2/D5	CKE	V11
IO28_L14N_2/D4	BA0	U10
IO37_L19P_2	BA1	AA15
IO38_L19N_2	A0	AB14
IO39_L20P_2	A1	U13
IO41_L21P_2	A2	Y13
IO42_L21N_2	A3	W14
IO45_L23P_2	A4	AB17
IO46_L23N_2	A5	AB18
IO48_L24N_2/D3	A6	Y15
IO60_L30N_2	A7	AB20
IO59_L30P_2	A8	AA20
IO51_L26P_2/D2	A9	Y18
IO52_L26N_2/D1	A10	Y19
IO50_L25N_2	A11	U15
IO49_L25P_2	A12	U14
IO35_L18P_2/GCLK2	CK	AB13
IO36_L18N_2/GCLK3	CK#	AA14
IO9_L5P_2	LOOPBACK_DQS	AB5
IO10_L5N_2	ST_LOOPBACK_DQS	AB6
IO62_L38N_3	LOOPBACK_CK#	U5
IO61_L38P_3	LOOPBACK_CK	U4
IO52_L33N_3	LDQS	V1
IO55_L35P_3	DQ0	Y1
IO56_L35N_3	DQ1	W1
IO53_L34P_3	DQ2	R3
IO54_L34N_3	DQ3	T4
IO47_L30P_3	DQ4	T1
IO50_L32N_3	DQ5	R5
IO45_L29P_3	DQ6	T6
IO46_L29N_3	DQ7	T5
IO48_L30N_3	LDM	U1
IO36_L22N_3	UDQS	N1
IO41_L26P_3	DQ8	P6
IO40_L25N_3	DQ9	P2
IO39_L25P_3	DQ10	P1
IO38_L24N_3	DQ11	N5
IO33_L21P_3/TRDY2/LHCLK6	DQ12	M6
IO34_L21N_3/LHCLK7	DQ13	N7
IO31_L20P_3/LHCLK4	DQ14	L3
IO32_L20N_3/LHCLK5	DQ15	M2
IO42_L26N_3	UDM	R6

Table 10: DDR – FPGA Pin Outs

The pins AB5 and AB6 are connected twice the length of data strobe signal. This is used for loop back the data strobe signal. The nets LOOPBACK_CK* are looped back twice the length of the Clock CK*. These loop backs are used for improving the performance of the DDR in micro blaze core.

The size of the memory can be increased to 64MB by using the MT46V32M16TG-6T from Micron (Drop & Replacement for existing part).

5.4. Communication

Spartan-3A DSP Reference Kit has access to an RS232 transceiver and Ethernet PHY transceiver for communication.

5.4.1. RS232 Transceiver

The RS232 transceiver LTC1331CG from Linear Technology is used in Spartan-3A DSP Reference Kit. This transceiver is operating at 3.3V. The internal charge pump creates the RS232 compatible output levels.

FPGA IO's are terminated to 3 driver / 5 receiver transceiver for debugging the board. A null modem cable should be used to plug “J2” into a standard PC serial port (male DB9). The standard pin outs of the RS232, which are interfaced to FPGA IO's, are shown in the following table.

Name	Signal Name	FPGA Ball No.
IP9_0	RD	D18
IO9_L4N_0	DSR	F16
IO10_L5P_0	CTS	E15
IO11_L5N_0	RI	F15
IO12_L6P_0/VREF2_0	TD	A16
IO13_L6N_0	RTS	A17
IO14_L7P_0	DTR	B20
IP12_0	DCD	E17

Table 11: RS232- FPGA Pin outs

Net Name	Transceiver Pin No.	DB9 (J1) Pin No.
DCD	8	1
DSR	9	6
RD	6	2
RTS	7	7
TD	5	3
CTS	10	8
DTR	11	4
RI	12	9

Table 12: RS232 Connector Pin outs

5.4.2. 10/100 Ethernet

The onboard Ethernet PHY KS8041NL requires single 3.3V supply 10base-T / 100base-TX physical layer transceiver, which provides MII interface to transmit and receive data. This is available in 32 Pin MLF Package. It has a built in 1.8V regulator for core. An RJ45 connector 5-6605869-7 from Tyco is used and it has two integrated LED's to show link and receive activity. Default PHY address is 00001.The Ethernet clock 25MHz is given from FPGA.

Name	Signal Name	FPGA Ball No.
IO58_L35N_1	MDIO	E20
IO13_L8P_1	RXDV	V22
IO14_L8N_1/VREF1_1	COL	U21
IO29_L18P_1/RHCLK0	REFCLK	N18
IO31_L19P_1/RHCLK2	MDC	N21
IO32_L19N_1/TRDY1/RHCLK3	TXC	M20
IO33_L20P_1/RHCLK4	RXC	L21
IO49_L30P_1/A18	CRS	G19
IO50_L30N_1/A19	TXD3	F20
IO51_L32P_1	TXD2	J19
IO52_L32N_1	TXD1	H20
IO53_L33P_1	TXD0	F22
IO54_L33N_1	TXEN	E22
IP9_L27P_1	RXD0/DUPLEX	J21
IP10_L27N_1	RXD1/AD2	J22
IP11_L31P_1/VREF7_1	RXD2/AD1	H21
IP12_L31N_1	RXD3/AD0	G20
IO47_L29P_1/A16	INTRP	K16
IO56_L34N_1	RESET#	G18
IO60_L36N_1/A21	RXER/ISOLATE	E19

Table 13: Ethernet PHY to FPGA Pin outs

5.4.3. Strapping Options

The strapping options provided in the Ethernet PHY are

nm	m	Isolate
R94	R85	Enable
R85	R94	Disable*

nm	m	Speed
R86	R92	100Mbps*
R92	R86	101Mbps

nm	m	Duplex
R83	R87	Half Duplex*
R87	R83	Full Duplex

nm	m	PHY Address
R79,R81,R91	R87,R89,R82	00000
R79,R81,R82	R87,R89,R91	00001*
R79,R89,R91	R87,R81,R82	00010
R79,R89,R82	R87,R81,R91	00011
R87,R81,R91	R79,R89,R82	00100
R87,R81,R82	R79,R89,R91	00101
R87,R89,R91	R79,R81,R82	00110
R87,R89,R82	R79,R81,R91	00111

*Default

Table 14: Strapping Options in Ethernet PHY

5.5. Analog to Digital Converter and Fast DAACs

The LTC2285 is a 14 bit 125 MSPS, low power dual 3V analog to digital converter designed for digitizing high frequency, wide dynamic range signals. SMA connector is used for giving analog (for both channels) and clock inputs. The digital output can be either in 2's complement format or offset binary format depending on mode pin.

The LTC2285 is perfect for demanding imaging and communication applications with ac performance that includes 72.2dB SNR and 82dB SFDR for signals at the nyquist frequency.

The input voltage to the analog to digital converter through the SMA Connector must be within +/- 1V input range. The input frequency ranges from 0.3MHz to 70MHz

Mode	Output Format	Clock Duty Cycle Stabiliser	Resistor	
			m	nm
0	Offset Binary	Off	R123	R120,R117,R114
1/3 VDD	Offset Binary	On	R120	R123,R117,R114
2/3 VDD	2's complement	On	R117	R123,R120,R114
VDD	2's complement	Off	R114	R123,R120,R117

Table 15: Mode Selection in ADC

A single 3V Supply allows low power operation. A separate output supply allows the output to drive 0.5V to 3.6V logic.

Fast DAACs Connector from MEC8-150-02-L-D-EM2 from SAMTEC is used for evaluating DC851 board (from Linear Tech) which will be plugged into it. The ADC will power off, when the add in card is inserted into the fast DAACs Connector. The I2C interface is used for communication between the DC851 board and Spartan-3A DSP reference Kit.

If the Spartan-3A DSP reference kit is used to acquire data from the DC851 board, the Spartan-3A DSP reference kit must be powered up before applying +3V across the pin marked "+3.0 V" and "GND".

.

Name	Signal Name	FPGA Ball No.
IO37_L18N_0/GCLK7	CLKOUT	B9
IO50_L25P_0	DA0	A6
IO48_L24P_0	DA1	B6
IP5_0	DA2	C5
IO51_L25N_0	DA3	A5
IO56_L28P_0	DA4	B4
IO46_L23P_0	DA5	G8
IO47_L23N_0	DA6	F9
IO54_L27P_0	DA7	F8
IO55_L27N_0	DA8	E8
IO45_L22N_0	DA9	D9
IO62_L31P_0/VREF5_0	DA10	E7
IO53_L26N_0	DA11	D7
IO43_L21N_0	DA12	D6
IP10_0	DA13	E6
IP13_0	DB0	F12
IO29_L14N_0	DB1	C12
IP2_0	DB2	A12
IP11_0	DB3	E10
IO33_L16N_0	DB4	D10
IO30_L15P_0	DB5	B11

IO31_L15N_0	DB6	A11
IP6_0	DB7	C10
IP1_0	DB8	A10
IO32_L16P_0	DB9	C9
IO44_L22P_0	DB10	C8
IO52_L26P_0	DB11	C7
IO49_L24N_0/VREF4_0	DB12	A7
IO42_L21P_0	DB13	C6
IO61_L30N_0	Input clock*	A3

Table 16: ADC to FPGA Pin Outs

Note: Remove the resistor R180 when the clock is applied through SMA Connector J5. Analog inputs are given through SMA Connector J3 and J4.

Name	Signal Name	FPGA Ball No.
IO1_0	ENABLE	H18
IO2_L1P_0	I2C_DATA	D19
IO34_L17P/GCLK4	I2C_CLOCK	A20

Table 17: FAST DAACs Connector to FPGA Pin outs

The pin out of SMA Connector is as follows:

Pin No	Signal Name
1	INPUT
2	GND
3	GND
4	GND
5	GND

Table 18: SMA Connector Pin outs

The Pin outs of the fast DAACs connector are as follows

Pin No	Signal Name	Pin No	Signal Name
1	GND	51	GND
2	AD13	52	GND
3	GND	53	GND
4	AD12	54	GND
5	GND	55	GND
6	GND	56	BD13
7	GND	57	GND
8	AD11	58	BD12
9	GND	59	GND
10	AD10	60	GND
11	GND	61	GND
12	GND	62	BD11
13	GND	63	GND
14	AD9	64	BD10
15	GND	65	GND
16	AD8	66	GND
17	GND	67	GND
18	GND	68	BD9
19	GND	69	GND

20	AD7	70	BD8
21	GND	71	GND
22	AD6	72	GND
23	GND	73	GND
24	GND	74	BD7
25	GND	75	GND
26	AD5	76	BD6
27	GND	77	GND
28	AD4	78	GND
29	GND	79	GND
30	GND	80	BD5
31	GND	81	GND
32	AD3	82	BD4
33	GND	83	GND
34	AD2	84	GND
35	GND	85	GND
36	GND	86	BD3
37	GND	87	I2C_CLK
38	AD1	88	BD2
39	GND	89	GND
40	AD0	90	GND
41	GND	91	I2C_DATA
42	GND	92	BD1
43	GND	93	POWER
44	GND	94	BD0
45	GND	95	GND
46	GND	96	GND
47	GND	97	BUS_ENABLE
48	GND	98	GND
49	GND	99	SENSE
50	CLK	100	GND

Table 19: Fast DAACs Connector

5.6. Radio Transceiver

The MICRF505 is a single chip, frequency shift keying transceiver intended for use in half duplex, bidirectional RF links .This multichannelled FSK transceiver is intended for UHF radio equipment in compliance with North American FCC. This is used in ISM Band (850 – 950 MHz) and the maximum data rate is 200KBaud.The clock 16 MHz is given from the FPGA.

The MICRF505 functions are enabled through a number of programming bits. There are 23 control registers in MICRF505 .The user can read all the control register and can write to the first 22 registers (0-21) and the register 22 is a read only register.

5.6.1. Control Interface

The control registers in MICRF505 are accessed through a 3-wire interface: Clock, data and chip select. These lines are referred to as SCLK, IO and CS respectively. This 3-wire interface is referred to as control interface.

5.6.2. Data Interface

Received data (via RF) and data to transmit (via RF) are handled by DataIXO and Dataclk (if enabled) lines. This is referred to as data interface.

The SCLK line is applied externally. Thus, the access to the control registers is carried out at a rate determined by the user. The MICRF505 will ignore transitions on the SCLK line if the CS line is inactive.

The frequency modulation can be done in two ways.
VCO Modulation (>20 Kbps)
Internal Modulation (<20 Kbps)

In this board VCO modulation is used. For this, the FPGA code need to Manchester encode the data that is sent to 505 on the DataIXO pin.

Name	Net Name	FPGA Ball No.
IO5_L3P_2	IO	W5
IO6_L3N_2	DATAIX0	Y4
IO7_L4P_2	CS	AB4
IO8_L4N_2	LD	AA4
IO9_L5P_2	RSSI	AB7
IO29_L15P_2/GCLK12	DATACLK	Y11
IO30_L15N_2/GCLK13	SCLK	Y10
IO32_L16N_2/GCLK15	XTALOUT	AB12

Table 20: Radio transceiver to FPGA pin outs

The antenna **S331AM-915** from **Nearson** can be used which has a frequency range of 902-928 MHz (ISM Band)

5.7. Stereo DAC

A stereo DAC AK4343EN from AKM is used to provide stereo line input and headphone out functions for this evaluation board. 2.5mm audio jack provides input and output connectivity.AK4343EN operates in PLL and external modes.
The 12 MHz clock is given from FPGA.

5.7.1. Control Interface

Internal registers are written by using the 3 wire interface pins (CSN , CCLK and CDTI) .The data on this interface consists of a 1-bit chip address (Fixed to 1), Read/write fixed to 1 , register address (MSB first , 6 bits) and control data (MSB first , 8 bits).Each bit is clocked in on the rising edge of CCLK. Address and data are latched on the 16^{th} CCLK rising edge after CSN falling edge. Clock speed of CCLK is 5MHz.The value of internal registers are initialized by PDN Pin = Low.

5.7.2. Audio Interface

Audio I/F interface includes LRCK, BICK and SDTI pins. Four types of data format are available and are selected by DIF 1-0 bits. In all the modes, the serial data is MSB first 2's complement format. Audio interface formats can be used in both master and slave modes. LRCK and BICK are output from AK4343 in master mode but must be input to AK4343 in slave mode.

Mode	Dif1 bit	Dif2 bit	SDTI (DAC)	BICK
0	0	0	DSP Mode	>= 32fs
1	0	1	LSB Justified	>= 32fs
2	1	0	MSB justified	>= 32fs
3	1	1	I^2S Compatible	>= 32fs

Table 21: Stereo DAC – Modes of Operation

The headers H8 and H9 are used to connect dynamic speaker and piezo speaker respectively. Mount the resistors R198 and R201 for connecting to dynamic speaker. Do not connect both the speakers at the same time. The minimum load resistance and load capacitance for the speakers are shown below.

Speaker Type	Dynamic Speaker	Piezo Speaker
Load Resistance (min)	8Ω	50Ω
Load Capacitance (max)	30pF	3µF

Table 22: Load resistance and capacitance of the Speaker

The minimum load resistance for the headphone output is 16Ω.

Name	Signal Name	FPGA Ball No.
IO36_L18P_0/GCLK6	MCKO	A9
IO39_L19N_0/GCLK9	I2C_SCL	E11
IO40_L20P_0/GCLK10	BICK	A8
IO41_L20N_0/GCLK11	LRCK	B8
IO57_L28N_0	CSN	A4
IO58_L29P_0	I2C_SDA	D5
IO59_L29N_0	PDN	C4
IO60_L30P_0	SDTI	B3
IO28_L14P_0	MCKI	C13

Table 23: Stereo DAC to FPGA Pin Outs

5.8. Video DAC

The ADV7125 has three separate 8 bit wide input ports. A single 3.3V power supply and clock are required to make the part functional. It has additional video control signals, composite sync # and blank# signals as well as power save mode.

This board provides a DB15 and video DAC to drive an RGB monitor. RGB output is output from FPGA in a 24-bit parallel format (8 bits each Red/Green/Blue). This data along with clock, blanking and synchronization signals is provided to ADV7125 DAC for Conversion to RS-343A/RS170 compatible video signals to drive an RGB monitor. The clock to video DAC is given from FPGA.

Clock	Resolution
25 MHz	640 X 480 (VGA)
50 MHz	800X600 (SVGA)
135 MHz	1280X1024(SXGA)

Table 24: Clock for Video DAC

Name	Net Name	FPGA Ball No.
IO41_L25P_1/A12	BLANK#	K20
IO28_L17N_1/A9	HSYNC	M22
IO46_L28N_1	PSAVE#	G22
IO42_L25N_1/A13	SYNC#	J20
IO27_L17P_1/A8	VSYNC	N22
IO30_L18N_1/RHCLK1	CLK_VIDEODAC	M17
IO16_L9N_1	BLUE0	T20
IO12_L7N_1	BLUE1	R20
IO11_L7P_1	BLUE2	R19
IO17_L10P_1	BLUE3	P19
IO8_L5N_1	BLUE4	T17
IO24_L14N_1/A5	BLUE5	P22
IO21_L13P_1/A2	BLUE6	N17
IO22_L13N_1/A3	BLUE7	P16

IO18_L10N_1	GREEN0	R18
IO10_L6N_1	GREEN1	Y22
IO9_L6P_1	GREEN2	W22
IO25_L15P_1/A6	GREEN3	N20
IO26_L15N_1/A7	GREEN4	N19
IO19_L11P_1	GREEN5	U22
IO15_L9P_1	GREEN6	U20
IO20_L11N_1/VREF2_1	GREEN7	T22
IO3_L2P_1/LDC1	RED0	Y21
IO5_L3P_1/A0	RED1	W19
IO6_L3N_1/A1	RED2	V20
IO4_L2N_1/LDC0	RED3	AA22
IO2_L1N_1/LDC2	RED4	U19
IO1_L1P_1/HDC	RED5	U18
IO7_L5P_1	RED6	T18
IO23_L14P_1/A4	RED7	R22

Table 25: Video DAC to FPGA Pin outs

A VGA Connector 1-1734530-3 from Tyco / XFATM9J-CTGG1-4M from XFMRS is used to connect a monitor from the Spartan-3A DSP Reference Kit to display the image captured by the camera module. The pin outs is shown below:

Pin No	Signal Name
1	RED
2	GREEN
3	BLUE
4	NC
5	GND
6	GND
7	GND
8	GND
9	5V
10	GND
11	NC
12	I2C_DATA
13	H_SYNC
14	V_SYNC
15	I2C_CLK

Table 26: VGA Connector Pin Outs

5.9. Camera Module

The VS6524 is a general purpose VGA resolution CMOS color digital camera featuring low size and low power consumption. It has an integrated 10 bit ADC, digital image processing functions including defect correction, lens shading correction, sharpening and color space conversion.

The VS6524 requires an analog power supply of between 2.4 V to 3.0 V and a digital supply of either 1.8V.An input clock is required in the range of 6.5 MHz to 26 MHz. The camera input clock is given from FPGA only. The default frequency is 12MHz.

Video data is output from VS6524 over a 8 bit parallel bus in RGB, YCbCr or Bayer formats and is controlled via I2C interface

The output formats supported are ITU-R BT.656-4 YUV (YCbCr) 4:2:2 with embedded syncs, RGB565, RGB444or Bayer 10-bit output formats.

YUV422 data format requires 4 bytes of data to represent 2 adjacent pixels and in RGB, Bayer output format two bytes of data are required for each output pixel.

All data output from VS6524 are qualified by pixel clock output. The pixel clock frequency is 24 MHz (equivalent to a 12 MHz pixel rate as each pixel is represented by 2 bytes of data).

This camera module is soldered on to ALPS Socket SCKA2A0100 which is on the board.

Name	Net Name	FPGA Ball No.
IO1_L1P_3	DATA0	F3
IO2_L1N_3	DATA1	G3
IO3_L2P_3	DATA2	C2
IO4_L2N_3	DATA3	C1
IO5_L3P_3	DATA4	F4
IO6_L3N_3	DATA5	F5
IO7_L5P_3	DATA6	H3
IO11_L7P_3	DATA7	G5
IO9_L6P_3	HSYNC	F2
IO10_L6N_3	VSYNC	F1
IO17_L11P_3	CE	G1
IO27_L18P_3/LHCLK0	CLOCK INPUT	L6
IO28_L18N_3/LHCLK1	PCLK	M5
IO2_L1P_0	I2C_DATA	D19
IO34_L17P/GCLK4	I2C_CLOCK	A20

Table 27: Camera Module to FPGA Pin outs

5.10. Displays

The Spartan-3A DSP reference kit uses LED and LCD displays for error and status indication.

5.10.1. On-Board Display

A LCD display module from TIANMA is included in this evaluation board. It has 20 characters X 2 lines text display and a 8 bit data bus. Backlighting can be turned on or off under program control using LCD_BKLT net routed to FPGA. The contrast of the display is adjusted by changing the resistor value R218.

Name	Net Name	FPGA Ball No.
IO34_L20N_1/RHCLK5	DATA0	L20
IO35_L21P_1/IRDY1/RHCLK6	DATA1	M18
IO36_L21N_1/RHCLK7	DATA2	L17
IO37_L22P_1/A10	DATA3	L22
IO38_L22N_1/A11	DATA4	K22
IO39_L24P_1	DATA5	K19
IO40_L24N_1	DATA6	K18
IO48_L29N_1/A17	DATA7	J17
IO59_L36P_1/A20	R/W# ENABLE	D20
IO61_L37P_1/A22	RS	D21
IO62_L37N_1/A23	BACKLIGHT	D22
IO43_L26P_1/A14	R/W# SELECT	H17

Table 28: LCD Module to FPGA Pin outs

5.10.2. LED

Eight discrete LED's are installed on the board and can be used to display the status of the internal logic. These LED's are lighted by forcing the associated FPGA I/O pin to a logic (1) and are off when the pin is either Low (0) or not driven.

Apart from the eight Discrete LED's, one more green and red LED's will indicate the status of the DONE Pin (after Configuration) and INIT pin (glows before and during configuration) of the FPGA respectively.

The Power on LED's for all power rails is green, which glows to indicate that all the power signals are stable.

Name	Net Name	FPGA Ball No.
IO15_L7N_0	LED0	A19
IO16_L8P_0	LED1	D15
IO17_L8N_0	LED2	C16
IO18_L9P_0	LED3	E13
IO19_L9N_0	LED4	D13
IO20_L10P_0	LED5	A14
IO21_L10N_0	LED6	B15
IO22_L11P_0	LED7	A13

Table 29 : LED to FPGA Pin Outs

5.10.3. DIP Switch and Push Button Switch

An eight-position dipswitch (SPST) has been installed on the board and attached to the FPGA. These switches provide digital inputs to user logic as needed. The signals are pulled down to logic low (0) by 100E ohm resistors when the switch is closed and tied to 2.5V (1) when the switch is open.

Name	Net Name	FPGA Ball No.
IP1_2	SWITCH0	AA6
IP2_2	SWITCH1	AB15
IP3_2	SWITCH2	W10
IP4_2	SWITCH3	Y6
IP5_2	SWITCH4	Y7
IP6_2	SWITCH5	Y12
IO16_L8N_2	SWITCH7	AA8
IO19_L10P_2	SWITCH6	V10

Table 30: DIP - FPGA Switch Pin Outs

One tactile switch form IIT cannon have been installed on the board and attached to the FPGA. This buttons can be programmed by the user and are ideal for logic reset and similar functions. It is at logic level high when it is not used.

Name	Push Button	FPGA Ball No.
IP3_0	SW1	A15
PROG#	SW5	A2

Table 31 : FPGA – Push Button Switch Pin Outs

The PROG# pin is an asynchronous control input to FPGA. When low, the PROG_B pin resets the FPGA, initializing the configuration memory. When released the PROG_B begins the configuration process. The initialization process does not start until PROG_B pin returns high.

5.11. IO Termination

There are two IO Pins that are terminated to header H10. These lines are having pulled up resistors. The header has power pins that can be used in future.

Name	Net Name	FPGA Ball No.
IO45_L28P_1	HD_T_DATA (H10.1)	H22
IO35_L17N_0/GCLK5	HD_T_CLOCK (H10.3)	F11

Table 32: FPGA to IO Termination Header

6. Clocks

The Spartan 3A DSP development kit includes a low cost PLL clock multiplier ICS501MLF from IDT. The synthesizer gets its input from a 10MHz crystal from Pletronics and then multiplies that input up to desired output frequency. The output frequency is selected by Jumper J11 and J12 according to Table shown below. The clock output from the synthesizer is delivered to the FPGA on the GCLK8 input at pin **F10**. The clocks to all the peripherals are derived from FPGA.

J12 (S1) Jumper Setting	J11 (S0) Jumper Setting	Multiplying Factor	Operating Frequency (MHz)
5-6(L)	5-6(L)	4	40
5-6(L)	3-4(M)	5.3125	53.125
5-6(L)	1-2(H)	5	50
3-4(M)	5-6(L)	6.25	62.5
3-4(M)	3-4(M)	2	20
3-4(M)	1-2(H)	3.125	31.25
1-2(H)	5-6(L)	6	60
1-2(H)	3-4(M)	3	30
1-2(H)	1-2(H)	8	80

Table 33: Output Frequency

7. FPGA Programming using iMPACT

7.1. Boundary scan

To Configure FPGA using Boundary scan, Xilinx parallel cable IV is used with ISE service pack 10.1i web pack, which can be downloaded from http://www.xilinx.com/support/download/index.htm. It is a high-speed downloadable cable that configures or programs Spartan FPGA. The Xilinx parallel cable IV is externally powered either to a power brick or to a standard PC mouse or keyboard connector. A Bi-color LED indicates the presence of operating and target reference voltage. If power is available and Vref detected, the color of status LED is Green and if power is available but Vref is not detected, the status LED color is changed to Amber. **Figure 6** indicates the LED status in Xilinx platform cable USB.

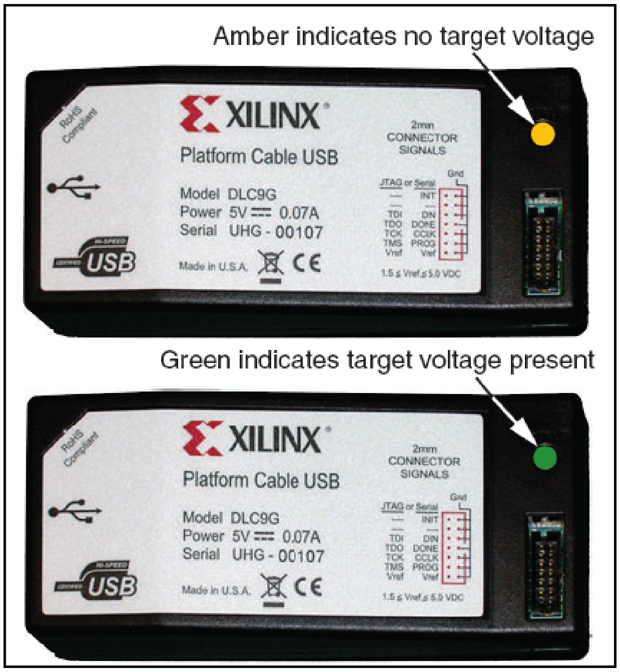

Figure 6: Status LED's indicating target Voltage

The following are the general steps to configure FPGA in JTAG mode.

1. The mode pin jumpers are set to JTAG mode as mentioned in **Section 5.2**(Install jumper on 2-3 pins of H2)

2. Open the impact software from start**->Programs -> Xilinx ISE Design Suite 10.1 -> ISE->Accessories -> IMPACT**. The following dialog box appears. Click **create a new project (.ipf**) and then click **OK.**

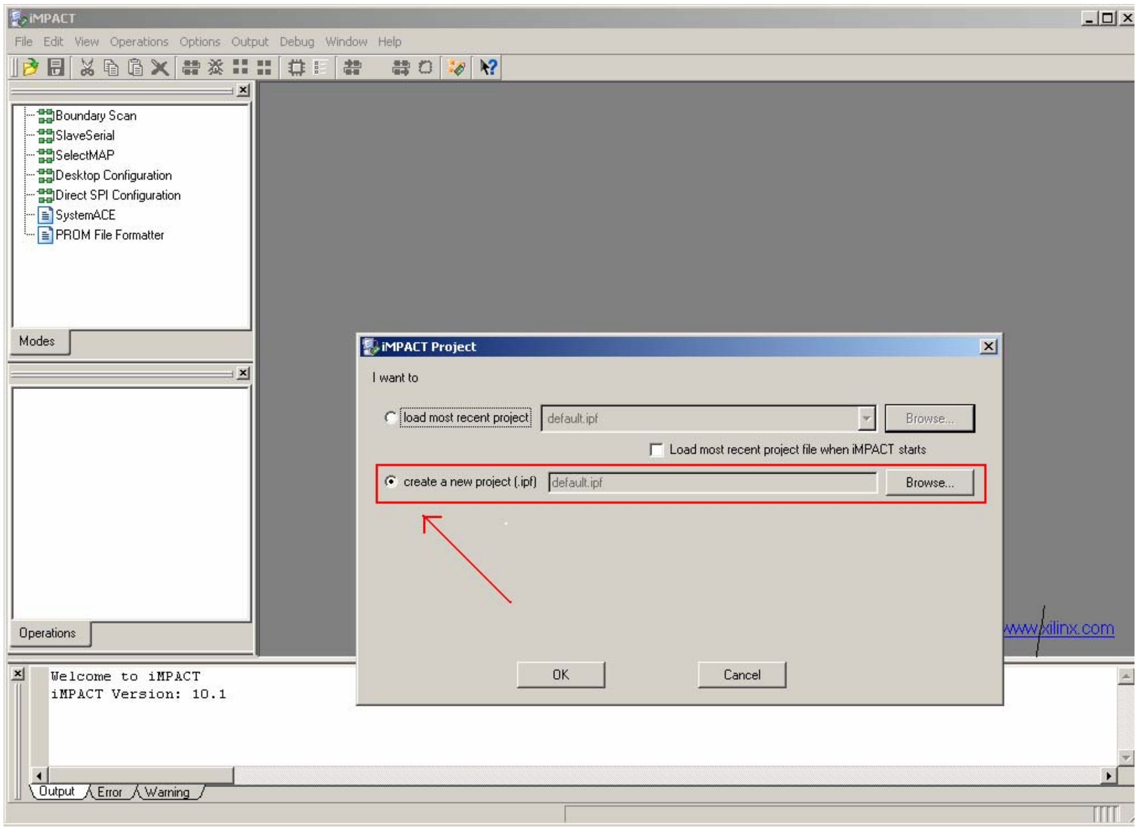

Figure 7: IMPACT Project window

3. The following window appears to choose the mode of configuration. Click the option button **configure devices using Boundary- scan JTAG (default)** and then click **Finish**.

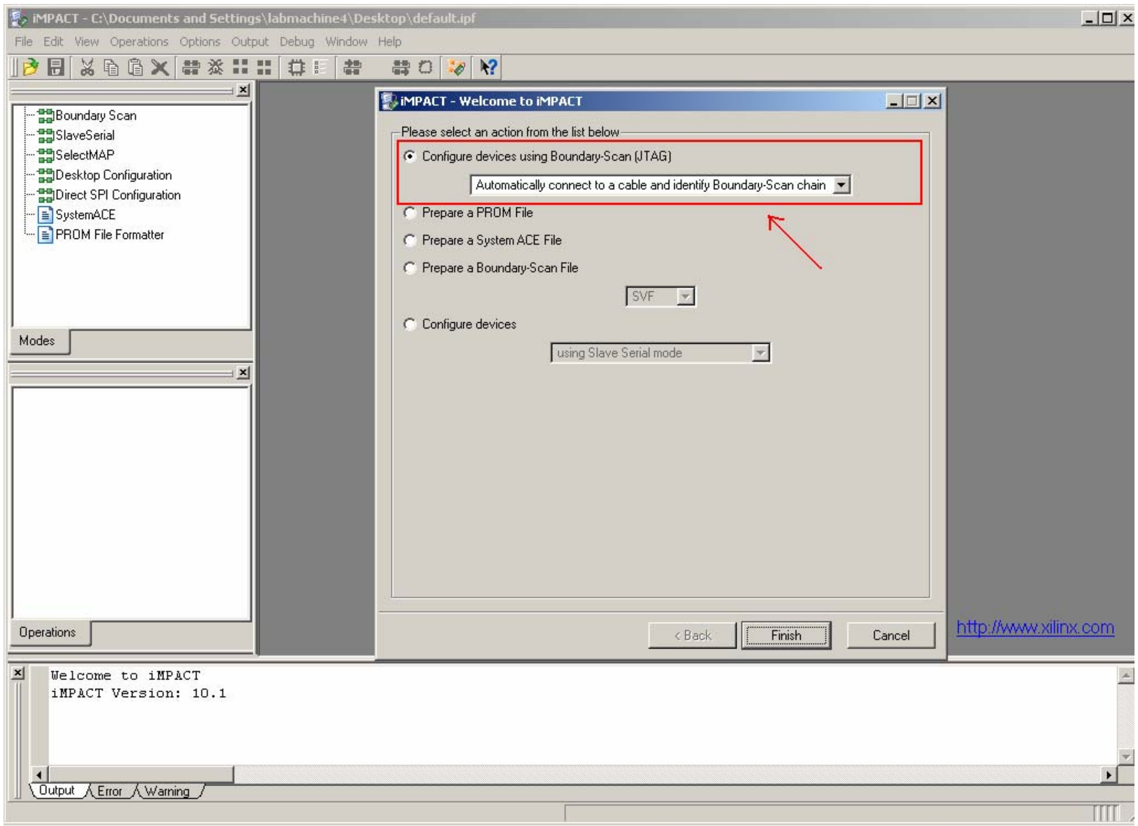

Figure 8: IMPACT configuration window

4. If the board is connected properly, the iMPACT programming software automatically recognizes the JTAG chain of Spartan 3A DSP as shown in the **Figure 9** and ask for the bit file to be programmed in the Spartan 3A DSP FPGA. Choose the corresponding bit file and click **open.**

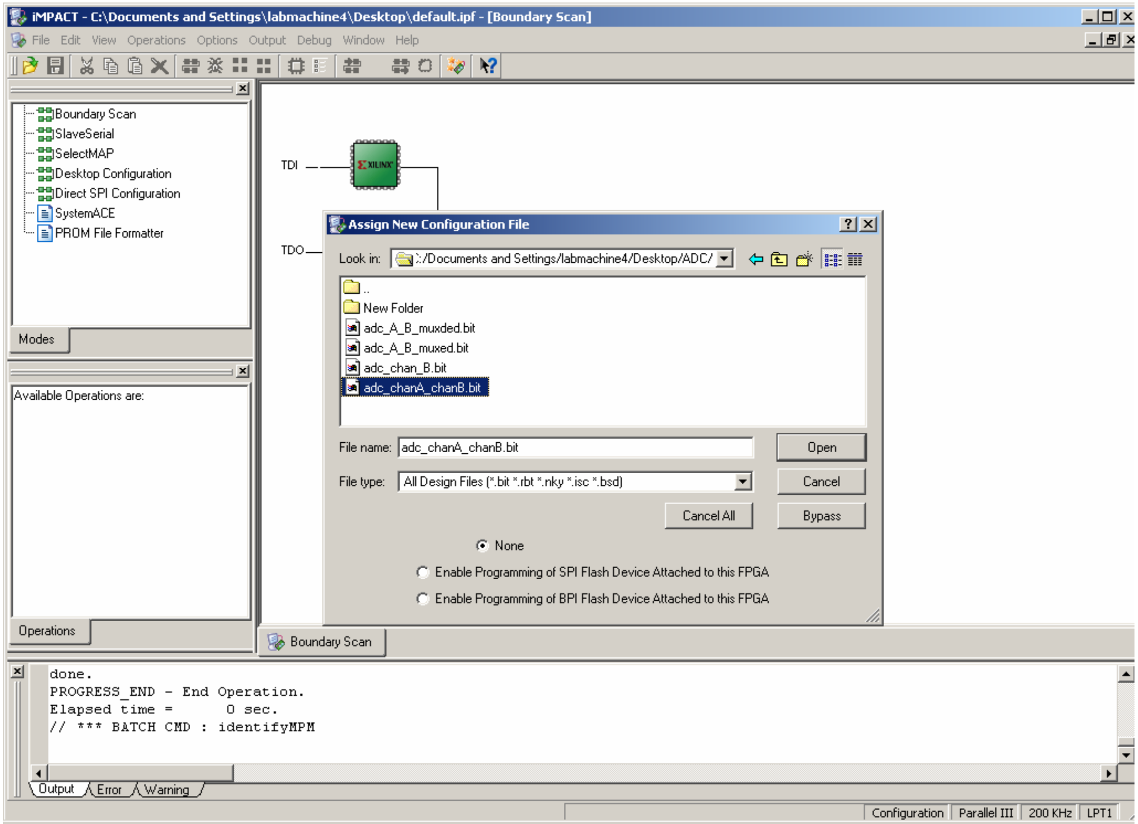

Figure 9: JTAG Chain

5. The programming properties window will open as shown below. Click ok to continue.

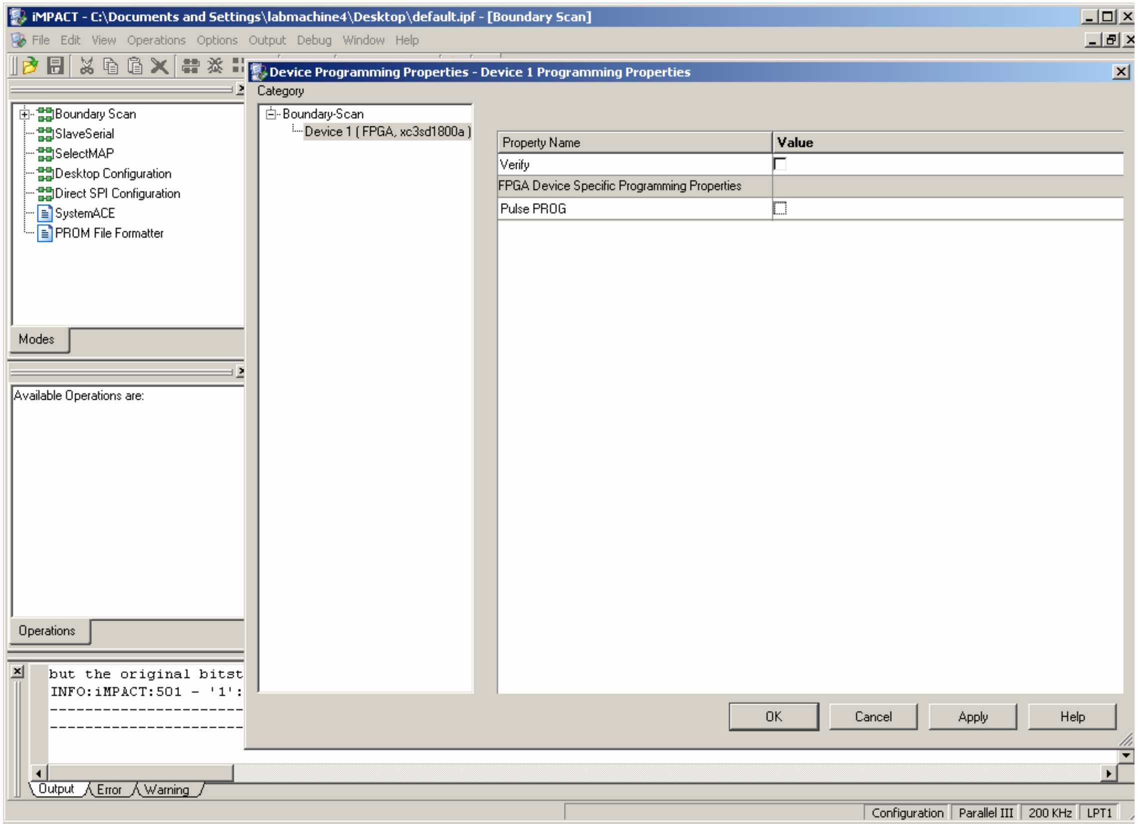

Figure 10: Device Programming Properties

6. Right Click the JTAG Chain and click **program** to continue.

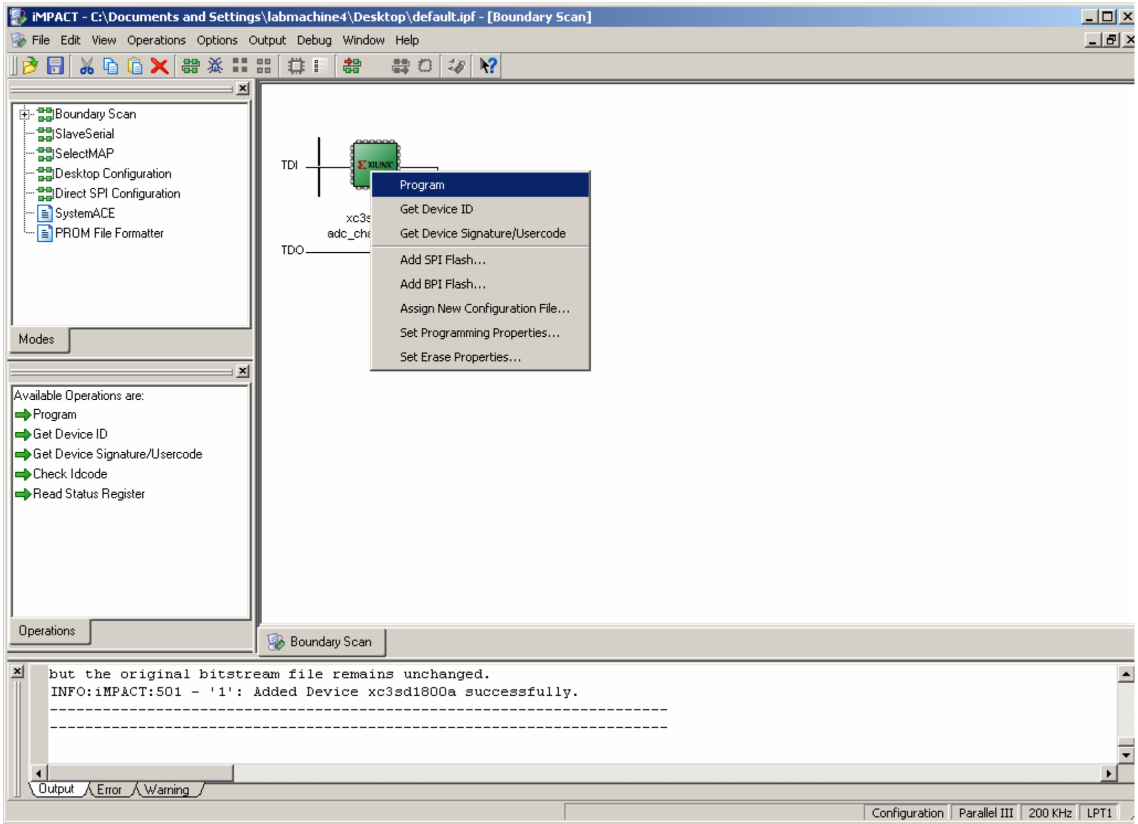

Figure 11: Programming the FPGA

JTAG programming to FPGA takes a few seconds depending on the speed of PC's USB port and iMPACT settings. A message appears displaying **Program succeeded** as shown below after successful programming.

The FPGA application is now executing on the Spartan 3A DSP board and the **DONE** pin LED glows when the FPGA is configured properly. The Impact software will display a message "Program succeeded" as shown below.

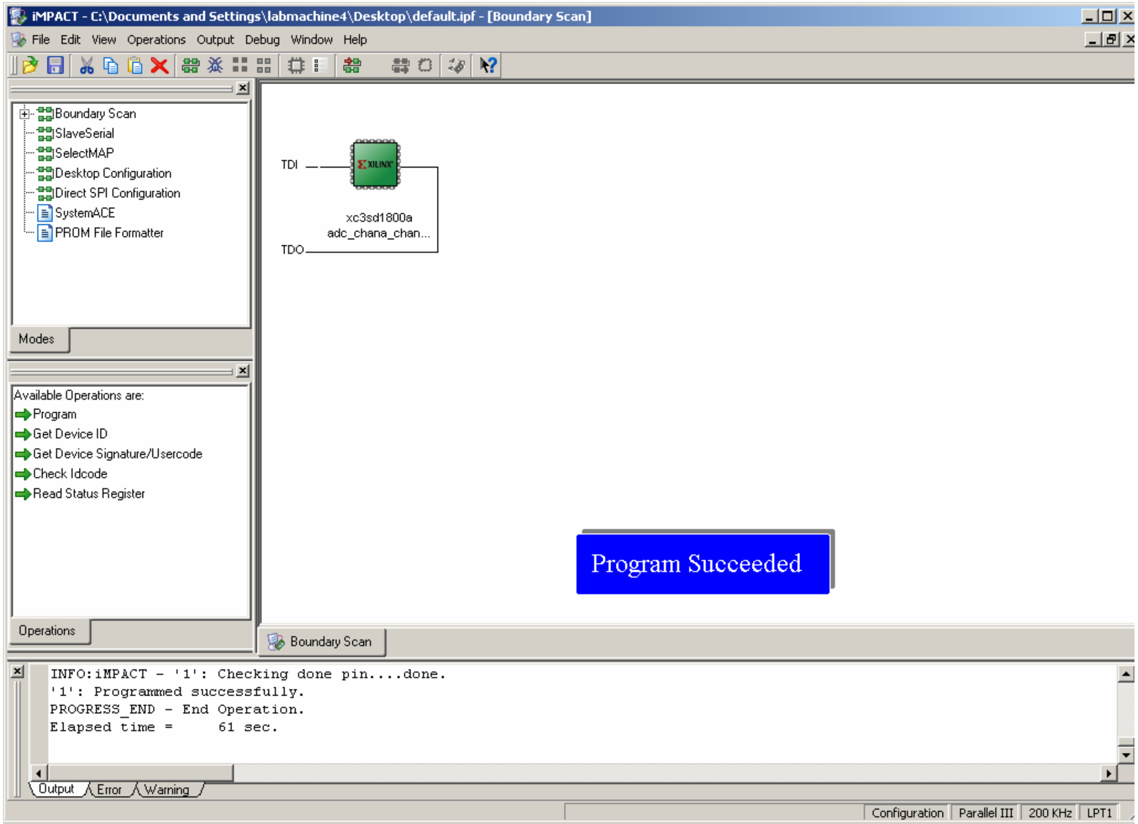

Figure 12: Program Succeeded

For Further information about configuring FPGA using JTAG refer http://www.xilinx.com/support/documentation/user_guides/ug332.pdf Spartan 3 generation user guide refer Page: 199

7.2. SPI Programming

To configure FPGA from SPI flash the mode select pins must set appropriately and SPI flash must contain a valid configuration file loaded. To load SPI configuration file (*.mcs) into the SPI flash using JTAG, indirect SPI programming and direct SPI programming method is used.

- Direct Method
- Indirect Method

For both these methods, PROM file (*.mcs) has to generated from the bit files. The following are the steps to generate the PROM file.

7.2.1. PROM File Generation

For configuring Spartan 3A DSP FPGA using SPI flash by direct or indirect method, PROM file has to be generated. The following steps are to be followed for generating PROM file:

1) Invoke **iMPACT**, and double click the PROM File formatter on the left tab of modes window. The following **iMPACT – Prepare PROM** files window will appear.

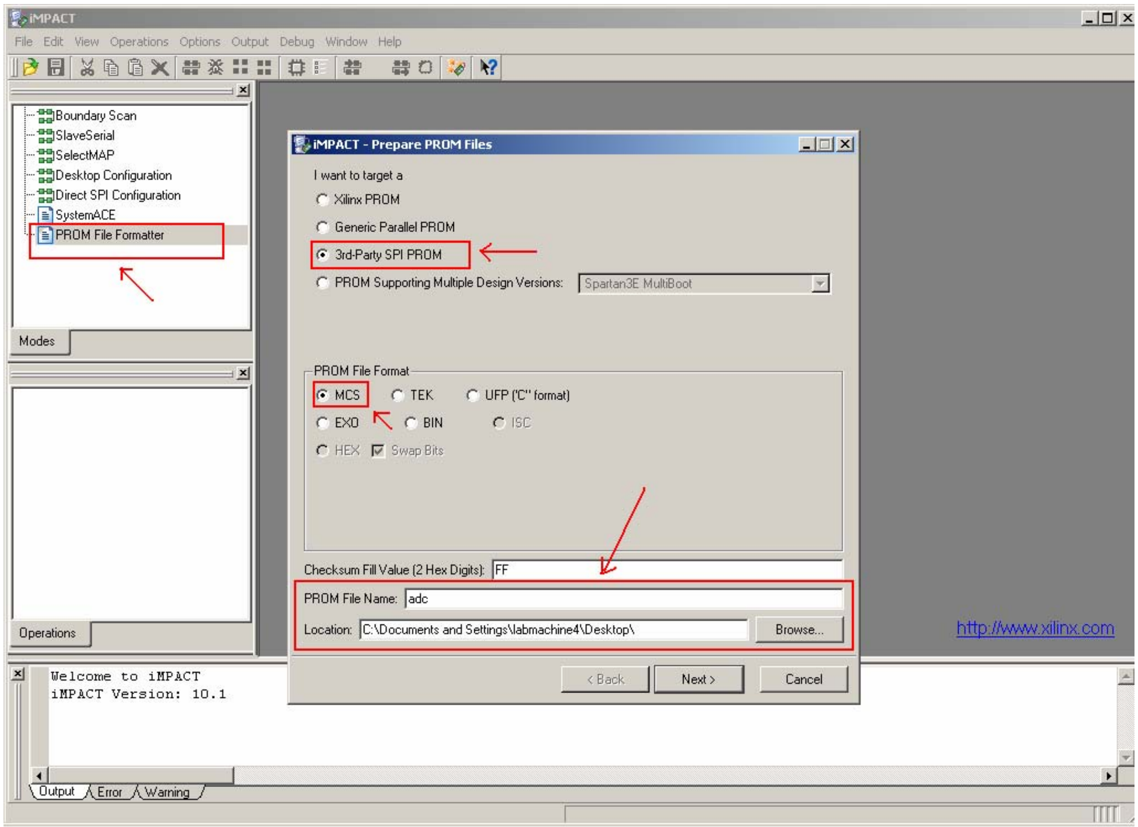

Figure 13: Prepare PROM Files dialog box

2) Click **3rd-party SPI PROM**, click **MCS** under **PROM File Format**, enter the **PROM File Name** as shown in the above figure, and then click **Next** to continue.

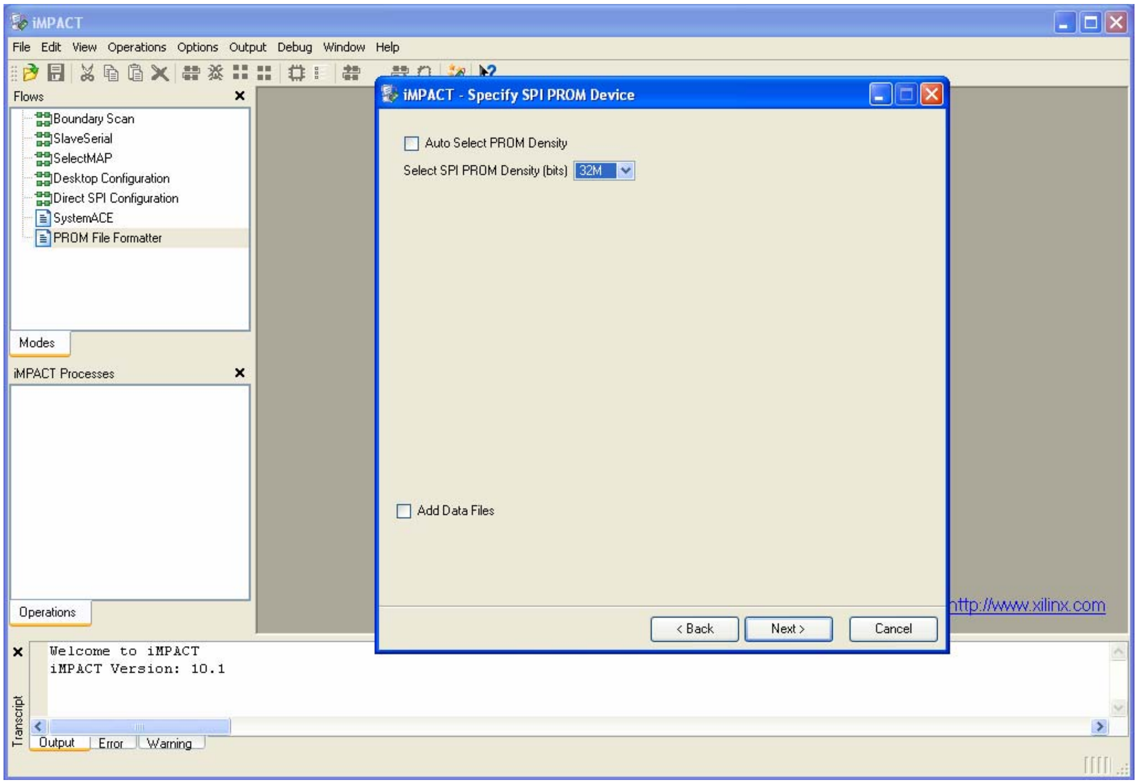

Figure 14: IMPACT – Specify SPI PROM Device window

3) Select **32M** in **Select SPI PROM Density** list, or check the **Auto Select PROM Density**, and then click **Next** to continue. It will generate the summary and finally click **Finish.**

4) The Pop- up message box appears displaying **Adding device to the SPI PROM** as shown in the below figure.

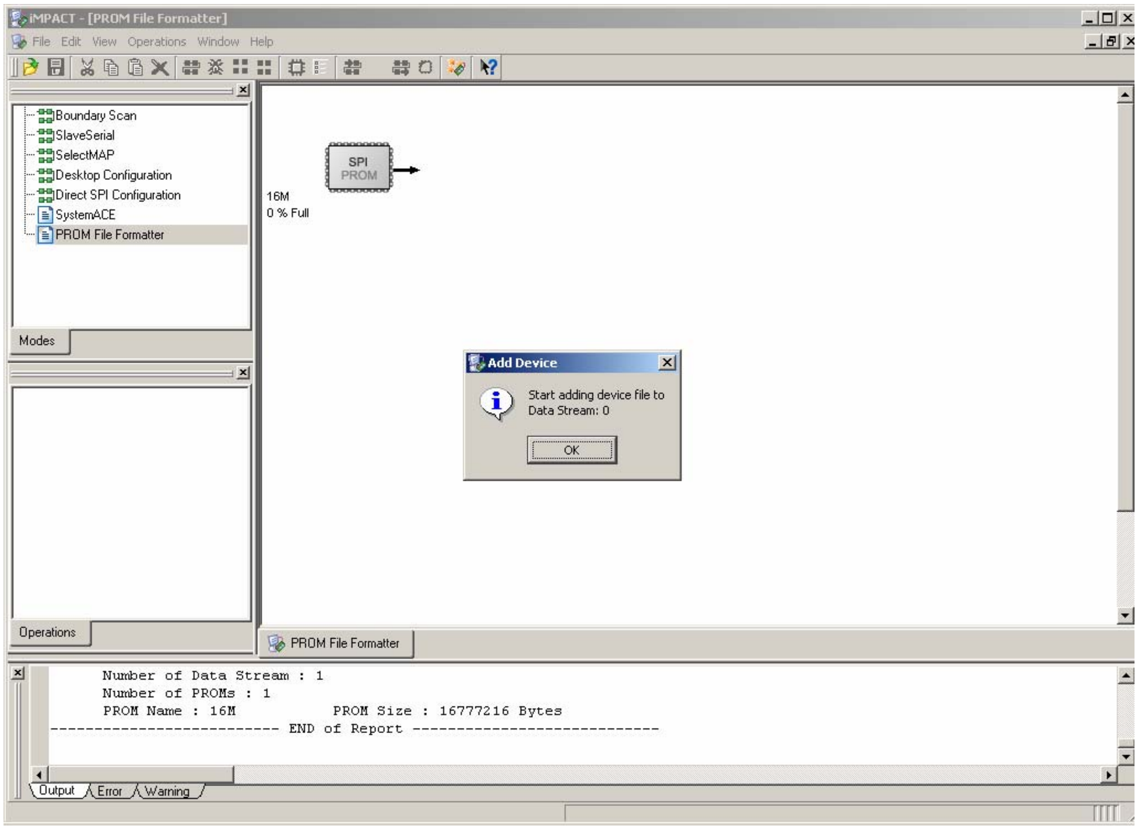

Figure 15: Adding Device to the SPI PROM

5) Click **OK** to add the BIT file to be converted to PROM format. Then click **No** to add any more devices.

6) Double-click the **Generate PROM file** in the left pane of **PROM File Formatter** tab in **IMPACT** window. The **PROM** file will be generated as shown in the figure below.

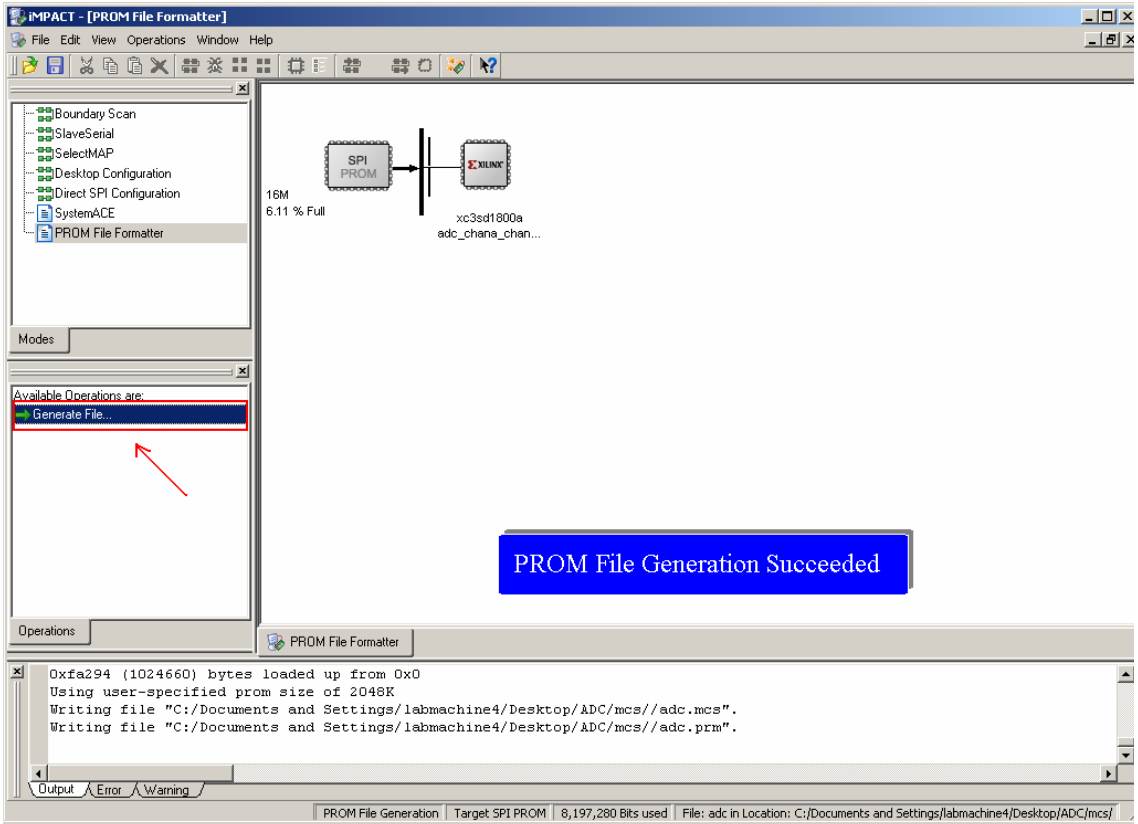

Figure 16: PROM file generation

7.2.2. SPI Flash Program: Indirect Method

These steps are to be followed after generating the PROM file to configure the flash using indirect method.

1) Connect the JTAG programming cable to FPGA's JTAG port H3.
2) Change the Mode pin jumper to the SPI mode.
3) Reapply the power to the board
4) In the **Boundary Scan** tab where JTAG chain is detected, right-click **Xilinx Spartan 3A-DSP**, and select **Add SPI Flash**. The **FPGA SPI Flash association** dialog box appears.
5) Select the Part Number for the attached SPI Flash PROM as **M25P128**.

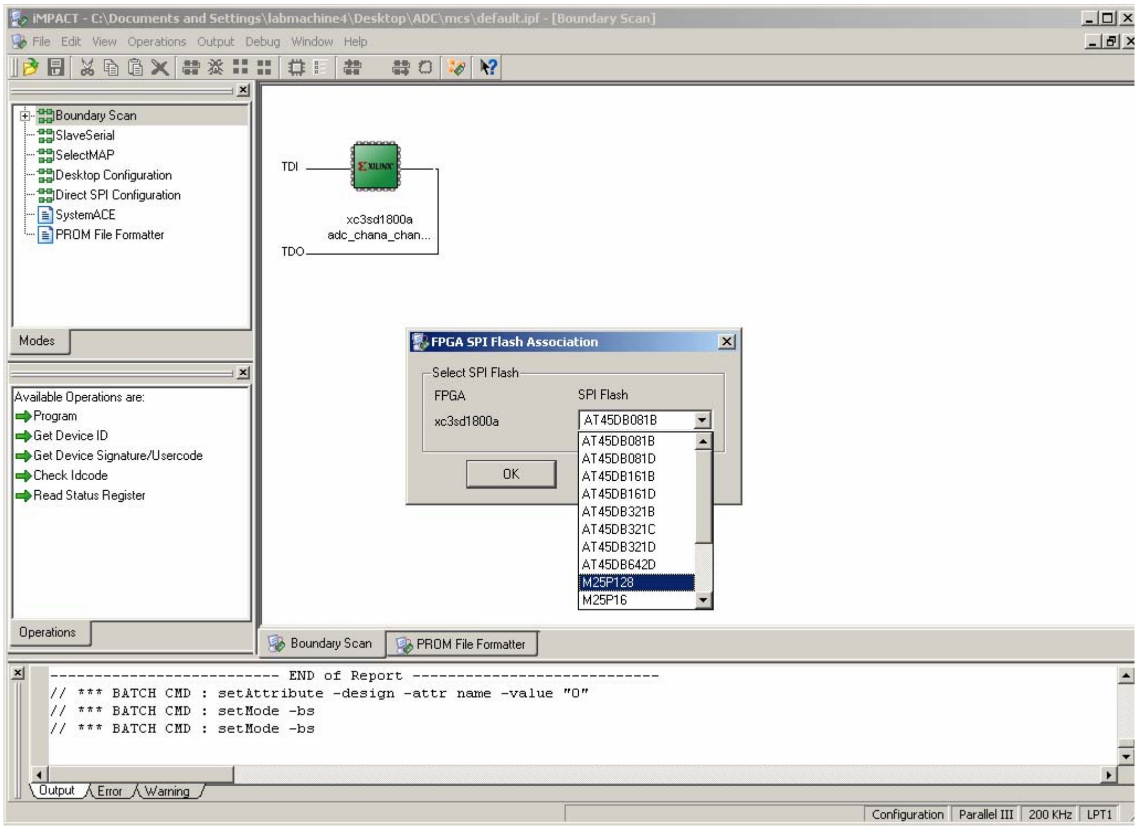

Figure 17 : Adding SPI Flash part number

6) The device programming properties window will appear. In that, select the Device 1 (Attached Flash , M25P128) in the boundary scan tab on the left side and make sure automatically load FPGA with Flash contents <default> is selected in After Programming Flash on the right side.

7) Right-click the **FLASH** device and select **ERASE**.

It takes few seconds to erase the SPI flash and IMPACT software will indicate with the message saying **ERASE SUCCEDED** as shown below.

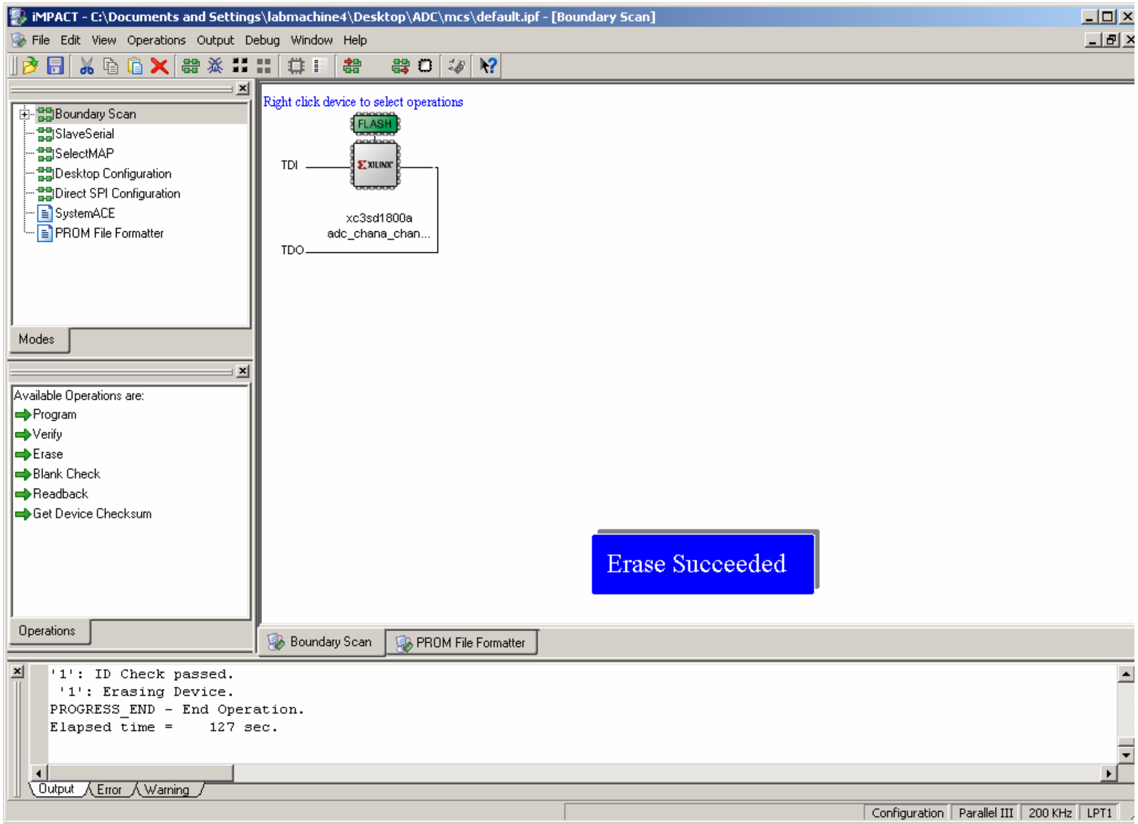

Figure 18: Erase Succeeded Message

8) Right-click Flash and select **Program**

It will take few minutes to Program the SPI flash and IMPACT software will indicate by displaying **PROGRAM SUCCEDED** message.

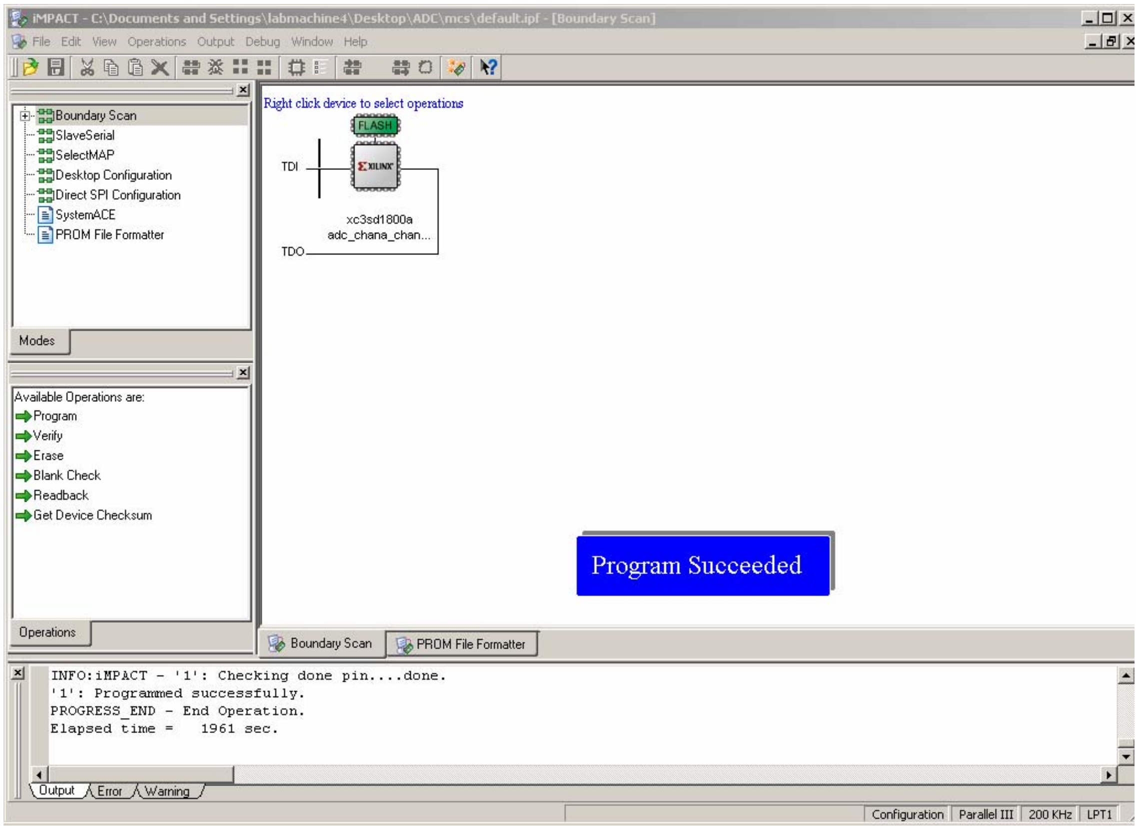

Figure 19: SPI Programming

The DONE LED will go high once the SPI flash is programmed.

9) Remove the JTAG programming cable

10) Power off the board and then power it again or press SW5.

11) Check Whether the DONE Led goes high.

12) Leave the Jumpers of the mode pins as SPI mode.

For further details about programming of SPI flash using indirect method using JTAG refer Page 120 of http://www.xilinx.com/support/documentation/user_guides/ug332.pdf Spartan 3 generation user guide

7.2.3. SPI Flash Programming: Direct Method

1. Disconnect the power to the board
2. Set the MODE pins of FPGA to Master SPI mode. This can be done by (Install jumper on 1-2 pins of H2)
3. Insert the jumper on 1-2 of J13 (FPGA_PROG#)
4. Connect the JTAG programming cable to FPGA's SPI Header H4.
5. Reapply the power to the board
6. Invoke IMPACT and select **configure devices.** Then select using direct SPI Configuration mode and click finish.

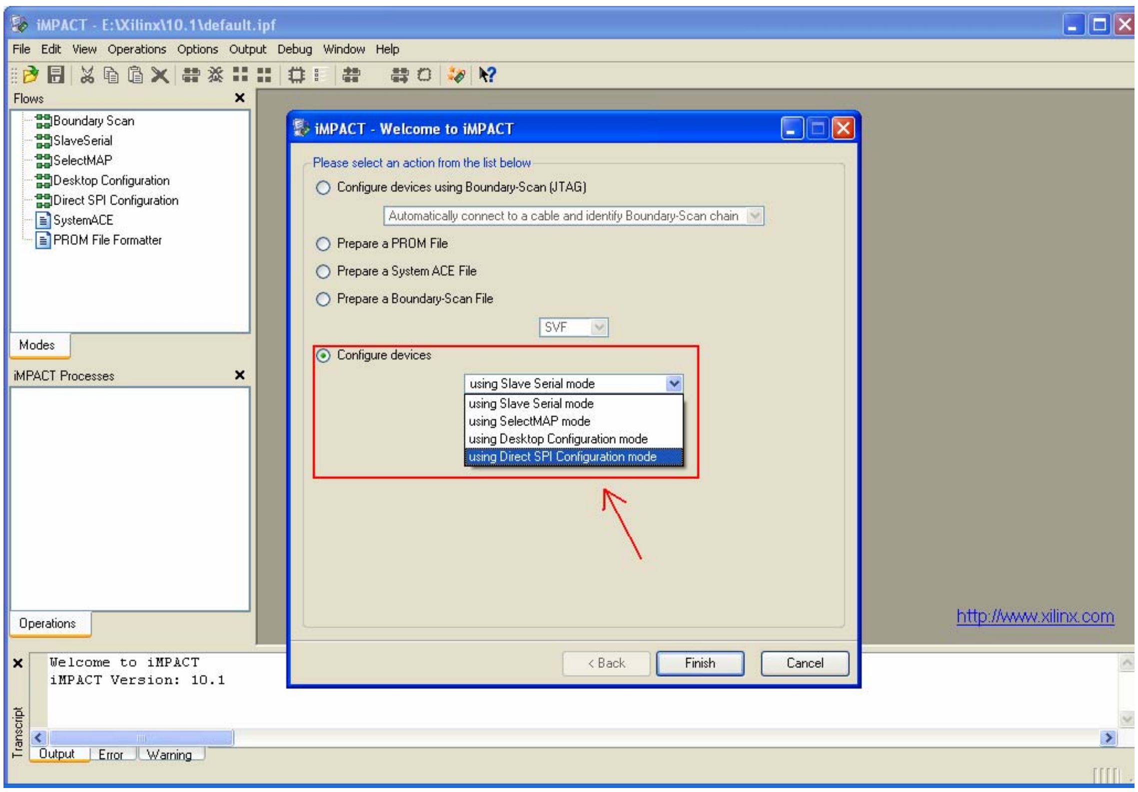

Figure 20: Select using direct spi programming mode

7. In the Next dialog Box select the .mcs file attached with the document and click **open** as shown below.

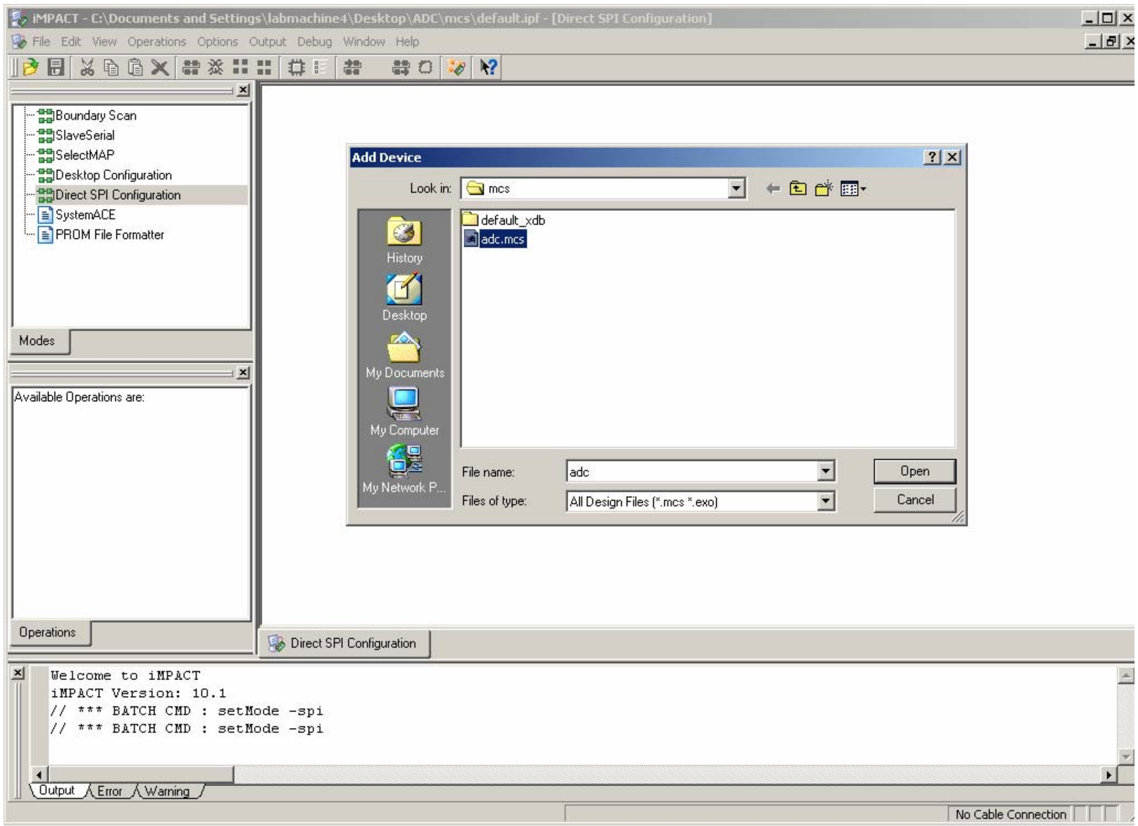

Figure 21: Selecting the .mcs

8. Then select **M25P128** in the select PROM. The select device part name dialog box is shown below.

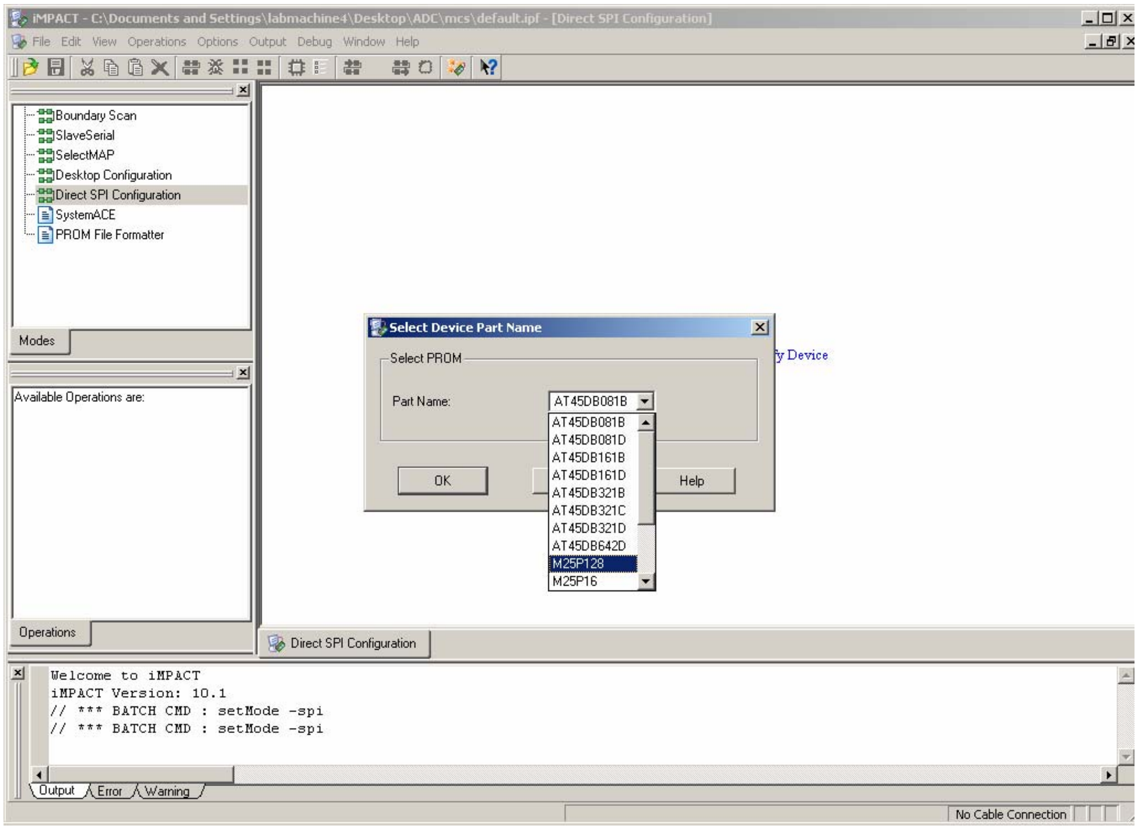

Figure 22: Selecting the SPI Flash

9. Right click the **FLASH** device and select **ERASE**

10. It will take few seconds to Erase the SPI flash and IMPACT software will indicate with the message saying **ERASE SUCCEDED.** The erase succeeded window is shown below.

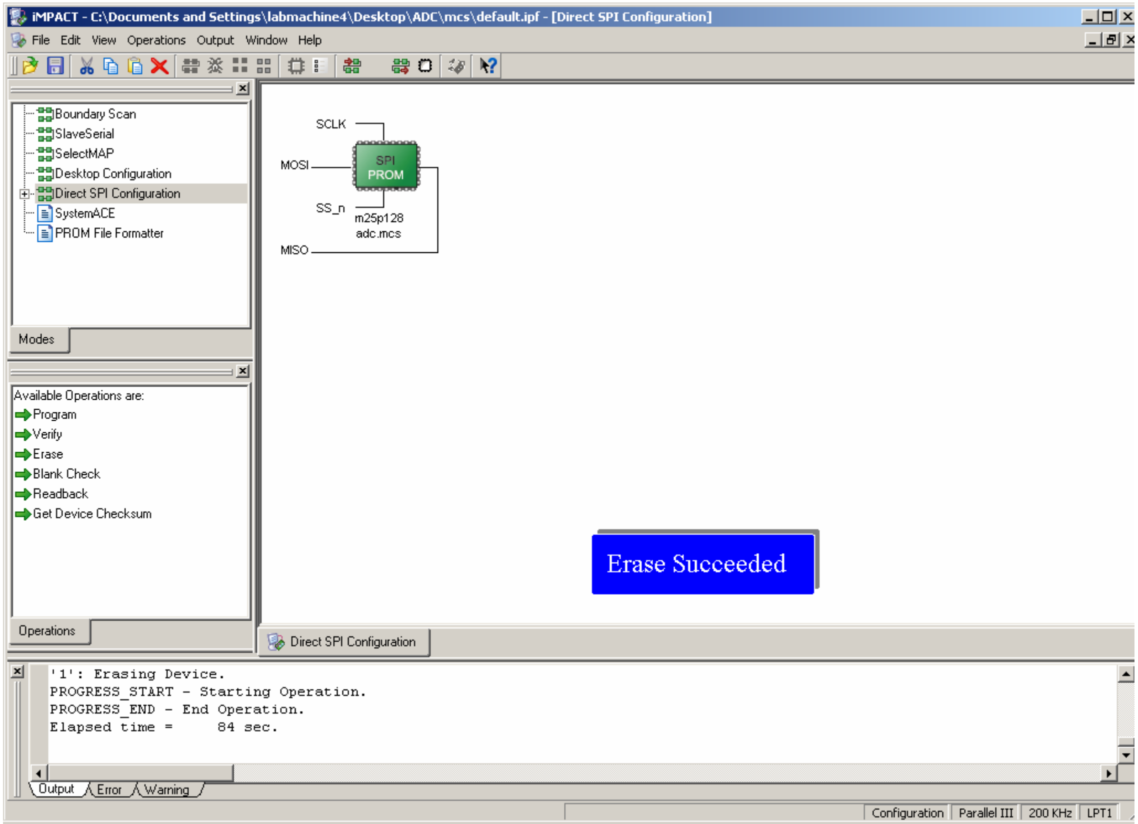

Figure 23: Erasing SPI Flash

11. Again Right Click the Flash and select **Program**

12. It will take few minutes to Program the SPI flash and IMPACT software will indicate with the message saying **PROGRAM SUCCEDED**

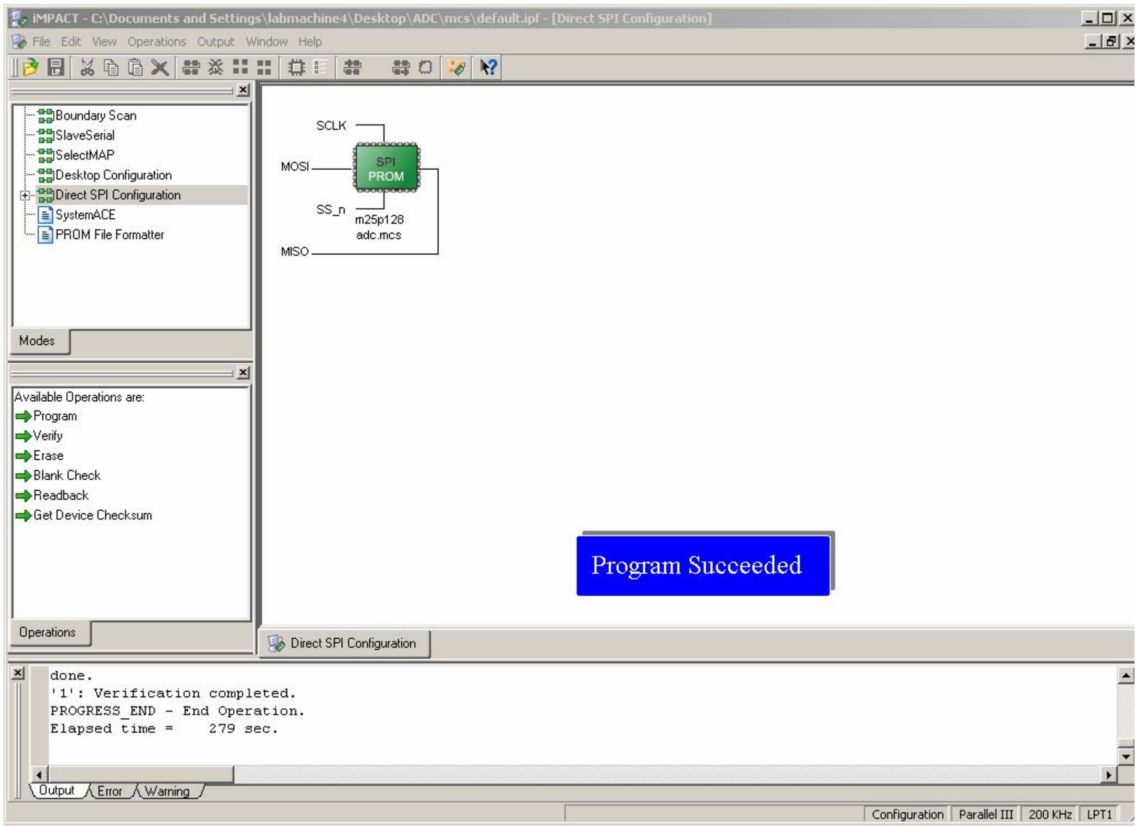

Figure 24: Programming the SPI Flash using direct method

13. Release the jumper on J13.
14. Remove the JTAG Programming cable on H4.
15. Reset the push button SW5 and the done led will glow.
16. Power off the board and then power it again or press SW5
17. Check Whether the DONE Led goes high.
18. Leave the Jumpers of the mode pins in the SPI mode itself.

For further details about programming of SPI flash using direct method refer Page 117 of http://www.xilinx.com/support/documentation/user_guides/ug332.pdf Spartan 3 generation user guide

8. References

The following publications contain related information

- Spartan-3A DSP Datasheet FPGA Family Datasheet
  http://www.xilinx.com/support/documentation/data_sheets/ds610.pdf
- Spartan-3 Generation FPGA User Guide
  http://www.xilinx.com/support/documentation/user_guides/ug331.pdf
- Spartan-3 Generation Configuration Guide
  http://www.xilinx.com/support/documentation/user_guides/ug332.pdf
- XtremeDSP-48A for Spartan-3A DSP FPGA's
  http://www.xilinx.com/support/documentation/user_guides/ug431.pdf

9. Abbreviation

Name	Abbreviation
SSTL	Stub Series Terminated Logic
RSDS	Reduced Swing Differential Signal
LVDS	Low Voltage Differential Signal
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVTTL	Low Voltage Transistor Logic
HSTL	High-Speed Transceiver Logic
DDR SDRAM	Double Data Rate Synchronous Dynamic Random Access Memory
SPI	Serial Peripheral Interface

Table 34: Abbreviation